
**PAS 9717/AO - SMT
ENGINEERING SPECIFICATION**

**8 CHANNEL, 16 BIT HIGH POWER
VME ANALOG OUTPUT CARD**
Rev B

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8 Channel 16 Bit High Power VME Analog Output Card

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8 Channel 16 Bit High Power VME Analog Output Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9717/AO-SMT provides eight high power analog output channels with sixteen-bit resolution on a 6U VME card. Each channel consists of a high speed Digital to Analog Converter, (DAC), followed by a high power operational amplifier. The output amplifiers are capable of supplying 50 mAmps of current, and will accept power supply voltages up to +/- 100 Volts. The total power dissipated by the amplifiers must be considered for each application to determine if the amplifier will drive the load. Example power dissipation calculations are shown in section IV of this specification.

All of the output channels and the external power supply connections can be terminated on the P2 connector of the VME backplane. A DB37 connector mounted through the front panel is available as an option for terminating the output and power supply signals. Refer to section II of this manual for ordering information.

The card can be used in VME systems with A16, A24, or A32 addressing, and data writes of 16 and 32 bits are supported. DIP switches are used to configure the width of the address bus, and the instruction type specifies the data bus width. A board identifier PROM, control and status register, and a 32-bit test register are also provided.

Card Features: PAS 9717/AO - SMT

- 8 independent DAC channels with 16 bit voltage outputs
- +/- 15 or +/- 40 Volt @ 50 mAmp output current
- Binary Two's Complement data format
- DAC's reset to bipolar zero during power up or software reset
- Output slew rate of 10 Volts per uSec
- Settling time of 12 uSec to 0.1% FSR
- Output signals and power supply terminate on P2 backplane connector, or on a DB37 connector at the front panel
- VME 6U form factor; 233 mm x 160 mm card size
- VME access: D32, D16, A32, A24, A16 Slave
- No VME Interrupts
- VME SYSFAIL asserts on power up, jumper selectable
- Board Identifier PROM (Board ID is VMEIDPAS9717AOB0)
- Pass, fail and board access LED's on the front panel
- Simultaneous DAC update feature is program selectable.
- Loop back test registers allow verification of the VME bus interface.
- 32-bit VME interface allows two channels to be written with one transfer and provides twice the data transfer rate of 16 bit interfaces. 16 bit VME transfers are also supported.
- DAC's are powered by the +/- 15 Volts from on board DC-DC converter.
- Operating temperature range 0 to 55 deg. C.

II. SPECIFICATIONS

Electrical Specifications	+/- 40 Volt Card	+/- 15 Volt Card
Number of Channels	8 Analog Outputs	8 Analog Outputs
Resolution	16 bits	16 bits
Output Voltage	+/- 40 Volts	+/- 15 Volts
LSB bit weight	1.22 mVolt	458 microVolt
Output Current	+/- 50 mAmps	+/- 50 mAmps
Current Limit	+/- 60 mAmps	+/- 60 mAmps
Output Resistance	75 ohms	75 ohms
Voltage Swing @ 40 mA	+/- (Vs –12 Volts)	+/- (Vs –12 Volts)
Settling Time	12 uSec to 0.1%(typ)	Same
PAS 9717/AO-X0Z	DAC7742Y (DAC Type)	
DAC Integral Nonlinearity T min. to T max.	+/- 5 LSB (max.) +/- 6 LSB (max.)	
DAC Differential Nonlinearity T min to T max.	+/- 4 LSB (max.)	
PAS 9717/AO-X1Z	DAC7742YB (DAC Type)	
DAC Integral Nonlinearity T min. to T max.	+/- 3 LSB (max.) +/- 4 LSB (max.)	
DAC Differential Nonlinearity T min. to T max.	+/- 2 LSB (max.)	
PAS 9717/AO-X2Z	DAC7742YC (DAC Type)	
DAC Integral Nonlinearity T min. to T max.	+/- 2 LSB (max.) +/- 3 LSB (max.)	
DAC Differential Nonlinearity T min. to T max.	+/- 1 LSB (max.)	
Zero Error	+/- 2 LSB (adjustable to zero)	
Gain Error	+/- 0.05 % FS (adjustable to zero)	
Card Power Requirements (Backplane power supplies)	5 Volts @ 1 Amp, (typ) 12 Volts @ N/A -12 Volts @ N/A	
External Power Supply		
Voltage	+/- 50 Volts (min), +/- 100 Volts (max)	
Quiescent Current	20 mA (typ.), 30 mA (max)	
Total Current	Quiescent current plus load current	

Environmental Specifications

Operating Temperature Range	0 to 55 degrees C.
Storage Temperature Range	-20 to 85 degrees C.
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	12 oz. (typ)
Connectors	2 ea. 96 position, (VME bus connectors) Analog Outputs on P2 a and c rows 1 ea. Optional DB37 female, (Analog Output connector)

Ordering Information

A three digit "dash number" specifies the configuration of the card. The three digits in the dash number are referred to as X, Y and Z. The dash number configurations are defined below.

X = 0; +/- 40 Volt Output

X = 1; +/- 15 Volt Output

Y = 0; Standard Linearity Grade DAC's

Y = 1; "B" Linearity Grade DAC's

Y = 2; "C" Linearity Grade DAC's

Z = 0; DAC and power supply terminate on P2

Z = 1; DAC and power supply terminate on DB37 at front panel

Valid Dash Number Combinations

+/- 40 Volt Card	+/- 15 Volt Card
000 = Standard DAC's, P2 I/O	100 = Standard DAC's, P2 I/O
001 = Standard DAC's, Front I/O	101 = Standard DAC's, Front I/O
010 = "B" Grade DAC's, P2 I/O	110 = "B" Grade DAC's, P2 I/O
011 = "B" Grade DAC's, Front I/O	111 = "B" Grade DAC's, Front I/O
020 = "C" Grade DAC's, P2 I/O	120 = "C" Grade DAC's, P2 I/O
021 = "C" Grade DAC's, Front I/O	121 = "C" Grade DAC's, Front I/O

Switches and Jumper Plug Definitions

The PAS 9717/AO-SMT card contains three eight position DIP switches, one three position DIP switch, and one jumper plug. The three eight position DIP switches are used to set the card's VME address and are defined in Table 1 below. When a switch is closed or on, the corresponding address bit must be low to select the card's address, and when a switch is open or off, the corresponding address bit must be high.

Switches SW4-1 and 2 are used to select the card's operating environment; A16, A24, or A32. The setting of these switches is defined in Table 2 on page 10.

Switch SW4-3 is used to enable the software reset function when it is open or off. Software reset is disabled when SW4-3 is closed or on. For more information on the software reset function, see the control and status register in the programming information section.

Jumper plug 2 controls the SYSFAIL line as described in the table 1.

TABLE 1
SWITCH AND JUMPER DEFINITIONS

<u>Switch #</u>	<u>Function</u>
SW1-1	A8
SW1-2	A9
SW1-3	A10
SW1-4	A11
SW1-5	A12
SW1-6	A13
SW1-7	A14
SW1-8	A15
SW2-1	A16
SW2-2	A17
SW2-3	A18
SW2-4	A19
SW2-5	A20
SW2-6	A21
SW2-7	A22
SW2-8	A23
SW3-1	A24
SW3-2	A25
SW3-3	A26
SW3-4	A27
SW3-5	A28
SW3-6	A29
SW3-7	A30
SW3-8	A31
JP2 IN	SYSFAIL controlled by control register

**TABLE 2
SWTICH DEFINITIONS**

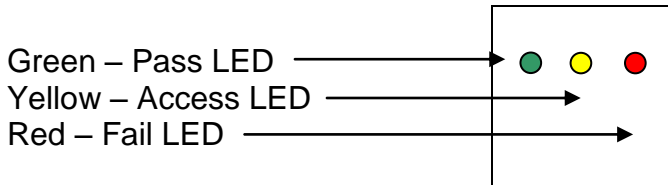
SW4-1	SW4-2	Address Modifiers	Address Space
Closed	Closed	09, 0D	Extended
Open	Closed	39, 3D	Standard
Closed	Open	29, 2D	Geographical *
Open	Open	29, 2D	Short

*Requires a special chassis

Front Panel LED Definitions

Three LED's are available at the front panel to indicate the board's status. The position of the LEDs is shown below.

Top of Front Panel



The Fail LED powers up on, and is controlled with bit 0 of the control register. Writing a one to bit 0 will turn off this LED. The state of this LED is reflected in bit 0 of the status register. When the Fail LED is on, and JP2 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the control register. This LED will be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the status register reflects the state of this LED. Once the board has passed some initial power up tests this LED can be turned on to indicate successful completion of the power up sequence.

The yellow, access LED will turn on anytime the board is accessed.

Connector Definitions

Two 96-position DIN connectors, (P1 and P2) are installed on the backplane end of the board to make the standard VME bus connection. The analog output signals and the external power supply connection can be made through the a and c rows of the P2 connector. An optional DB37 female connector, installed through the board's front panel, is available to provide front access to the eight analog output channels, and the power supply connections. When the DB37 connector is installed, jumpers are removed so the analog outputs and power supply are not connected to P2.

The pin definitions of P2 and the DB37 connector are defined below and on the following page.

TABLE 3
P2 Connector

AGND	P2a1	P2c1	OUTPUT 0
AGND	P2a2	P2c2	OUTPUT 1
AGND	P2a3	P2c3	OUTPUT 2
AGND	P2a4	P2c4	OUTPUT 3
AGND	P2a5	P2c5	OUTPUT 4
AGND	P2a6	P2c6	OUTPUT 5
AGND	P2a7	P2c7	OUTPUT 6
AGND	P2a8	P2c8	OUTPUT 7
AGND	P2a9	P2c9	EXT V+
AGND	P2a10	P2c10	EXT V-

TABLE 4
OPTIONAL DB37 CONNECTOR

AGND	37	19	N/C
AGND	36	18	N/C
AGND	35	17	N/C
AGND	34	16	N/C
AGND	33	15	N/C
AGND	32	14	N/C
AGND	31	13	N/C
AGND	30	12	N/C
AGND	29	11	N/C
AGND	28	10	OUTPUT 0
AGND	27	9	OUTPUT 1
AGND	26	8	OUTPUT 2
AGND	25	7	OUTPUT 3
AGND	24	6	OUTPUT 4
AGND	23	5	OUTPUT 5
AGND	22	4	OUTPUT 6
AGND	21	3	OUTPUT 7
AGND	20	2	EXTV+
		1	EXTV-

III. PROGRAMMING INFORMATION

The 9717/AO - SMT card responds to word and longword writes to the eight Digital to Analog Converters (DAC's). The card also supports word writes and reads to the control and status register, and word reads of the board identifier PROM. A thirty two-bit test register is provided, and it responds to word and longword transfers. This register is useful for verifying the functionality of the VME bus interface. The card's memory map is shown below.

TABLE 5

PAS 9717/AO-SMT MEMORY MAP

00	00	V (56)	01
02	00	M (4D)	03
04	00	E (45)	05
06	00	I (49)	07
08	00	D (44)	09
0A	00	P (50)	0B
0C	00	A (41)	0D
0E	00	S (53)	0F
10	00	9 (39)	11
12	00	7 (37)	13
14	00	1 (31)	15
16	00	7 (37)	17
18	00	A (41)	19
1A	00	O (4F)	1B
1C	00	B (42)	1D
1E	00	0 (30)	1F
20	97	17	21
22	Control & Status	Control & Status	23
24	Test Register	Test Register	25
26	Test Register	Test Register	27
28	Reserved	Reserved	29
3E	Reserved	Reserved	3F
40	CH 0	CH 0	41
42	CH 1	CH 1	43
44	CH 2	CH 2	45
46	CH 3	CH 3	47
48	CH 4	CH 4	49
4A	CH 5	CH 5	4B
4C	CH 6	CH 6	4D
4E	CH 7	CH 7	4F

Board Identifier PROM (Base Address + 00H to 1EH) Read Only

The Board Identifier PROM is located starting at the board's base address plus 0, and continues to the base address plus 1E. Byte and word reads to the Identifier PROM are supported.

Only the least significant byte of a word read will contain valid data, and the most significant byte will contain 00. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

Fast ID Register (Base Address + 20H) Read Only

The fast ID register is located at the card's base address plus 20. Reads to this register will return the hex value 9717, which is the board's model number. Writing this register will handshake, but not transfer any data.

Control and Status Register (Base Address +22) Read / Write

The Control and Status Register (CSR) is located at the cards base address plus 22. Writes to the control register are used to set the states of the LED's and the SYSFAIL line, to control the simultaneous update function, and to software reset the board. The word format of the CSR is shown below.

TABLE 6

Control and Status Register

15	14 through 5	4	3	2	1	0
Loop Back HT	Loop Back HT	Loop Back HT	SW Reset Pulse	Sim Updat HT	Pass LED HT	Fail LED LT

LT = Low True

HT = High True

Bit 0 of the CSR steers the Fail LED and the SYSFAIL line on the backplane, if J1 is installed. When the card is reset the Fail LED will come on, and the SYSFAIL line will be driven true. Writing a one to bit 0 will turn off the LED and the SYSFAIL line.

Bit 1 of the CSR controls the Pass LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 will turn on the LED.

Bit 2 of the CSR controls the simultaneous update feature. This function is disabled when the board is reset or when a zero is written to bit 2. When simultaneous update is disabled, the DAC outputs will updated when they are written to.

Simultaneous update is used to update all of the DAC outputs at the same time, and is controlled with bit 2. The program sequence for updating the outputs simultaneously is described below in the section on the D to A converters.

Bit 3 in the Control Register controls the software reset function when enabled by SW4-3 being open. When bit 3 is written with a one with reset enabled, the reset pulse will be generated. Software reset causes all the DACs to reset to zero volts, and clears the CSR and Test Register to all zeros. When the software reset function is disabled, bit 3 has no function, other than to loop back the value that was written last.

Bits 4 through 15 of the CSR are loop back bits, and will return the value that was last written to them.

The power up or reset condition of the CSR is 0000, and indicates, that simultaneous update is disabled, the Pass LED is off, and the Fail LED is on.

Test Register (Base Address + 24) Read / Write

The 32-bit Test Register can be written to and read at the card's base address plus 24 (hex). This register supports word and long word transfers, and is useful for verifying the proper operation of the VME bus interface. Reading the register will return the value that was last written to it.

D to A Converters (Base Address + 40) Write Only

The eight Digital to Analog Converters, (DAC's), are addressed starting at the board's base address plus 40 (hex). Binary Two's Complement is the data format written to the DAC's. Writing a value of 7FFF (hex) to a DAC produces positive full-scale output on that channel. Writing a value of 8000 (hex) produces negative full-scale output, and 0000 (hex) produces zero output.

Dual rank register pairs are used in the DAC's so that they can be updated simultaneously. Data is always written into the DAC's input register, which is the first register in the pair. If the simultaneous update feature is disabled, the second register, known as the DAC register, will also be updated during the write. This causes the output voltage for that channel to change immediately during the write.

When the DAC's are updated simultaneously, all of the DAC input registers are written, then the card is instructed to update all the DAC registers. This causes all of the outputs to change at the same time.

The following sequence is performed to cause the outputs to update simultaneously;

- 1) Bit 2 in the CSR is set to a one to disable the DAC registers from tracking the

- input registers,
- 2) All of the DAC input registers are written to,
 - 3) Bit 2 in the CSR is set to zero. This causes all of the DAC outputs to update.

The Digital to Analog Converters can be written individually using word transfers, or in pairs using longword transfers. After a power up or software reset, the output voltage of all of the DAC's is 0.000 Volts.

IV. AMPLIFIER CIRCUIT DESCRIPTION

The PAS 9717/AO-SMT card contains eight high power amplifier circuits driven by high resolution D to A converters. All of the amplifier circuits have gain and offset adjustments. A calibration procedure is provided on the following page, and describes how to make these adjustments.

The amplifiers used on this card are high voltage monolithic MOSFET operational amplifiers. They deliver performance features previously only found in hybrid designs, while increasing reliability. The amplifier part number is PA241, and they are built by Apex Microtechnology Corporation.

The PA241 is packaged in Apex's hermetic SIP10 package. This package has a typical thermal resistance of 55 degrees Celsius per Watt from junction to air, and the device has a maximum junction temperature of 150 deg. C. Based on these parameters, the amplifier will dissipate a maximum of 1.7 Watts, and should typically be operated at 1.25 Watts or less.

When the amplifier is configured to drive 60 Volts at 50 mAmps into a resistive load with +/- 75 Volt power supplies, the maximum power in the amplifier will be 1.17 Watts. In this example, the load resistance is 1.2 K Ohms, and the maximum power dissipation in the amplifier occurs at half of the power supply voltage.

Under these conditions, the power in the amplifier is calculated to be,
 $(37.5 \text{ Volts} \times 37.5 \text{ Volts}) / 1.2 \text{ K Ohms} = 1.17 \text{ Watts}$

As the output voltage increases from this point, the voltage across the amplifier decreases, and as the output voltage decreases, the current through the amplifier and the load decreases. When the amplifier is driving this load to 60 volts, it is delivering 3 Watts of power to the load, and the amplifier is dissipating 750 mWatts.

When the amplifier is configured to drive 40 Volts at 50 mAmps into a resistive load with +/- 52 Volt power supplies, the maximum power in the amplifier will be 0.845 Watts. In this example, the load resistance is 800 Ohms, and the maximum power dissipation in the amplifier occurs at half of the power supply voltage.

Under these conditions, the power in the amplifier is calculated to be,
 $(26 \text{ Volts} \times 26 \text{ Volts}) / 800 \text{ Ohms} = 845 \text{ mWatts}$

Other factors to consider when using these cards are that the amplifiers require a minimum of +/- 50 Volt power supplies and the power supply voltages must be 12 Volts greater than the output voltage swing. This voltage is required to properly bias the current sources in the amplifiers, so that they will meet their published specifications. In applications where the amplifier always has a positive output voltage and delivers the load current from the positive supply, a negative power supply with a low output current can be used. The low current negative supply is always required to properly bias the internal current sources.

V. CALIBRATION PROCEDURE (+/- 40 Volt Option)

Install the 9717/AO-SMT card in a VME chassis, and connect the external power supply of at least +/- 50 Volts to the card. Allow the card to stabilize for approximately 2 minutes.

Offset Adjustment

The offset adjustment is performed before the gain adjustment to avoid interaction of adjustments. Write the hex value 0000 to the channel being calibrated, and adjust the zero potentiometer for a value of 0.0000 Volts. The zero adjustments are defined in the Table 7, below.

Gain Adjustment

Write a hex value of 7FFF to the channel being calibrated, and adjust the gain potentiometer for a value of + 39.9988 Volts. The gain adjustments are the defined in Table 7, below. Write the hex value 8000 to the channel being calibrated and verify the output voltage is -40.000 volts.

TABLE 7
OFFSET AND GAIN ADJUSTMENT POTS

P3 Pin Number	Channel Number	Offset Pot	Gain Pot	Channel Address
10	0	8	12	40
9	1	17	21	42
8	2	26	30	44
7	3	35	39	46
6	4	44	48	48
5	5	53	57	4A
4	6	62	66	4C
3	7	71	75	4E

V. CALIBRATION PROCEDURE (+/- 15 Volt Option)

Install the 9717/AO-SMT card in a VME chassis, and connect the external power supply of at least +/- 50 Volts to the card. Allow the card to stabilize for approximately 2 minutes.

Offset Adjustment

The offset adjustment is performed before the gain adjustment to avoid interaction of adjustments. Write the hex value 0000 to the channel being calibrated, and adjust the zero potentiometer for a value of 0.0000 Volts. The zero adjustments are defined in the Table 7, below.

Gain Adjustment

Write a hex value of 7FFF to the channel being calibrated, and adjust the gain potentiometer for a value of + 14.9995 Volts. The gain adjustments are the defined in Table 7 below. Write the hex value 8000 to the channel being calibrated and verify the output voltage is -15.000 volts.

TABLE 7
OFFSET AND GAIN ADJUSTMENT POTS

P3 Pin Number	Channel Number	Offset Pot	Gain Pot	Channel Address
10	0	8	12	40
9	1	17	21	42
8	2	26	30	44
7	3	35	39	46
6	4	44	48	48
5	5	53	57	4A
4	6	62	66	4C
3	7	71	75	4E