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PAS 9723/AI
ENGINEERING SPECIFICATION

32 CHANNEL SIMULTANEOUS SAMPLING
12 BIT VME ANALOG INPUT CARD
Revision B (03/13/2003)

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32 Channel Simultaneous Sampling
12 Bit VME Analog Input Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9723/AI provides thirty-two, simultaneous sampling, twelve bit, analog input channels on a 6U format VME card. VME systems with A16, A24, or A32 addressing are supported, and data reads of 16 bits are used to access the input channels. DIP switches are used to configure the width of the address bus.

This card includes thirty-two, individual, differential input, precision amplifiers. Each amplifier drives a corresponding sample and hold stage, which, upon receipt of a common trigger signal, “freezes” the output of the differential amplifier. Each amplifier has a standard gain of 1.000, but has provisions for the installation of a precision gain setting resistor to increase the front end gain by as much as 1,000:1.

The sample and hold stages are followed by a 32 channel scanning analog multiplexer, that drives the input of a 12 bit Analog to Digital Converter. Switch selectable full-scale ranges of 0 to +10.24V, 0 to +5.12V, +/- 10.24 V or +/- 5.12Vare available. A 32 word by 16 bit data register file and VME interface are provided for storing the results of the A to D conversions and making them available to the VME bus.

The analog input signals are terminated on a pair of 37 position female D-sub connectors mounted through the front panel. The external trigger signal is provided with a Lemo type RA00 female coaxial connector.

When the card is not scanning and converting data, all of the track and hold amplifiers will be tracking the amplified analog input signals. Upon receipt of an external trigger signal, the card will hold the value of all the analog input signals, and initiate an acquisition scan. Using the sequential multiplexer, the A/D converter will acquire and digitize all 32 channels, and write the results of each conversion into the proper register location. During this scan sequence, VME register access is limited.

Two front panel LED’s are provided to indicate the card’s status. An amber Scan LED will flash whenever the module is triggered. A blue VME LED will light whenever the card is accessed from the VME bus.

Additional features include, a board identifier PROM, and a control and status register.

Card Features: PAS 9723/AI

- 32 simultaneous sampling analog voltage input channels
- 32 channel scanning analog multiplexer and 12 bit A/D Converter
- Instrumentation Amplifier per channel with resistor programmable gain
- Selectable +/- 10.24 V, +/- 5.12 V, 0-10.24 V, or 0 to 5.12V, input voltage ranges
- Left justified offset binary data format, four LSB's return zeros
- VME 6U form factor; 233 mm x 160 mm card size
- VME access: A32, A24, A16; D16 Slave
- No VME Interrupts
- Optional VME SYSFAIL assert on power up, jumper selectable
- Scan and board access LED's on the front panel
- Board Identifier PROM (Board ID is VMEID PAS9723/AI A0)
- Analog input signals terminate on a pair of DB 37 connectors at the front panel
- External trigger input signal terminates on a coax connector at the front panel
- Operating temperature range 0 to 60 deg. C

II. SPECIFICATIONS

Electrical Specifications

Number of Channels	32 Analog Inputs, 1 External Trigger Input
Resolution	12 bits
Input Voltage Ranges	+/- 10.24 Volts, +/- 5.12 Volts 0 to 10.24 Volts, 0 to 5.12 Volts
Input Impedance	1000 M ohms II 6 pF (typ)
Input Bias Current	500 pAmps (typ)
Over Voltage Protection	+/- 40 Volts
Max. Settling Time	5 uSec (typ) to 0.01%
ADC Integral Nonlinearity	+/- 1 LSB (max.)
ADC Differential Nonlinearity	+/- 1 LSB (max.)
Offset Error	+/- 2 LSB
Full Scale Error	+/- 2 LSB
External Trigger Rate	6 KHz Max (Note 1)
External Trigger Input	TTL Level input with 1K Ohm pull-up to +5 V
Card Power Requirements	5 Volts @ 2 Amps, (typ)

Environmental Specifications

Operating Temperature Range	0 to 60 degrees C.
Storage Temperature Range	-20 to 85 degrees C.
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	12 oz. (typ)
Connectors	2 ea. 96 position, (VME bus connectors) 2 ea. DB37 female, (Analog Input connectors) 1 ea. External trigger coax connector

Note 1: Multiplexing and conversion takes 5 uSec per channel, therefore scanning all 32 channels requires 160 uSec

Switches, Jumpers and Indicators

The 9723/AI card contains four DIP switches, two jumper plugs and two LED indicators. Three of the DIP switches are used to set the board's VME base address, and are defined in the table 1 on page 9. When a switch is closed, the corresponding address bit must be low to select the card's address. When a switch is open, the corresponding address bit must be high. The card is shipped configured for address C000.

Switches 2-9 and 2-10 are used to select the boards operating environment, either A16, A24 or A32, and the setting of these switches is defined in table 1 on page 9. The card is shipped configured for short space, SW2-9 and 10 are both open.

Switches SW4-1 through SW4-4 are used to select the input voltage range of the card, as defined in table 2 on page 10. The card is shipped configured for +/- 10.24 volt inputs, SW4-1 through 4 are all closed.

Switches SW4-5 through SW4-8 are used to select the source of the trigger signal as defined in table 3 on page 10. All of these switches enable their respective function, when they are closed. SW 4-5 and SW 4-6 are used to select either the positive or negative edge of an external trigger pulse to initiate a scan sequence. SW-6 enables an on board 2 KHz generator to initiate scan sequences, and is intended only for logic testing. Only one of these switches should be enabled at a time, and none should be enabled, if software or global triggering is used. S4-8 enables a 2 uSec low pass filter to be applied to the external trigger signal. This filter is useful in electrically noisy environments, to prevent false triggering. The card is shipped configured for software trigger, SW4-5 through 8 are all open.

Note: The internal 2KHz trigger signal is not functional at this time.

Jumper JP1 is removed for shipping and is reserved for future use.

Jumper JP2 is used to select the source of the 16 MHz clock. When it is installed in position 1-2, an on-board oscillator supplies the clock. When JP2 is in position 2-3 the clock is supplied from the backplane. The card is shipped with JP2 in position 2-3.

TABLE 1

DIP SWITCH DEFINITIONS

Switch #	Function
SW1-1	A6 (not used)
SW1-2	A7
SW1-3	A8
SW1-4	A9
SW1-5	A10
SW1-6	A11
SW1-7	A12
SW1-8	A13
SW1-9	A14
SW1-10	A15
SW2-1	A16
SW2-2	A17
SW2-3	A18
SW2-4	A19
SW2-5	A20
SW2-6	A21
SW2-7	A22
SW2-8	A23
SW3-1	A24
SW3-2	A25
SW3-3	A26
SW3-4	A27
SW3-5	A28
SW3-6	A29
SW3-7	A30
SW3-8	A31
SW2-9 closed, S2-10 closed	A32 Addressing
SW2-9 closed, S2-10 open	A24 Addressing
SW2-9 open, S2-10 open	A16 Addressing

TABLE 2

Input Voltage Range Switches

SW4-1	SW4-2	SW4-3	S4-4	Range
Closed	Closed	Closed	Closed	+/- 10.24 V
Closed	Closed	Closed	Open	+/- 10.24 V
Closed	Closed	Open	Closed	+/- 10.24 V
Closed	Closed	Open	Open	+/- 10.24 V
Closed	Open	Closed	Closed	+/- 10.24 V
Closed	Open	Closed	Open	+/- 10.24 V
Closed	Open	Open	Closed	0 to 5.12 V
Closed	Open	Open	Open	+/- 10.24 V
Open	Closed	Closed	Closed	+/- 10.24 V
Open	Closed	Closed	Open	+/- 10.24 V
Open	Closed	Open	Closed	0 to 10.24 V
Open	Closed	Open	Open	+/- 5.12 V
Open	Open	Closed	Closed	+/- 10.24 V
Open	Open	Closed	Open	+/- 10.24 V
Open	Open	Open	Closed	+/- 10.24 V
Open	Open	Open	Open	+/- 10.24 V

TABLE 3

Trigger Signal Source Switches

SW4	5 Trigger on Positive Edge
SW4	6 Trigger on Negative Edge
SW4	7 Internal Trigger (not implemented)
SW4	8 Filter Trigger Signal

Two LED’s are provided at the front panel to indicate the board's status. The blue LED indicates the board is being accessed by the VME bus. The yellow LED indicates the board is in the process of sampling and converting data.

Connector Definitions

Two 96 position DIN connectors are installed on the back plane end of the board to make the standard VME bus connection. A pair of DB37 female connectors are installed through the board's front panel to provide access to the thirty-two analog input channels. A right angle PC mount Coax connector is provided between the DB37 connectors to provide access to the external trigger input signal. The pin out of these connectors is defined below and on the following page.

External Trigger Connector, P5	Lemo P/N: EPS.00.250.NTN
Cable Mating Connector	Lemo P/N: FFA.00.250.CTAC31

Pin #	Signal Name
1	External Trigger In
2	Ground

TABLE 4

DB37 Connectors P4

		19	N/C
AGND	37		
		18	AGND
IN15-	36		
		17	IN15+
IN14-	35		
		16	IN14+
IN13-	34		
		15	IN13+
IN12-	33		
		14	IN12+
IN11-	32		
		13	IN11+
IN10-	31		
		12	IN10+
IN9-	30		
		11	IN9+
IN8-	29		
		10	IN8+
IN7-	28		
		9	IN7+
IN6-	27		
		8	IN6+
IN5-	26		
		7	IN5+
IN4-	25		
		6	IN4+
IN3-	24		
		5	IN3+
IN2-	23		
		4	IN2+
IN1-	22		
		3	IN1+
IN0-	21		
		2	IN0+
AGND	20		
		1	AGND

TABLE 5

DB37 Connectors P3

		19	N/C
AGND	37		
		18	AGND
IN31-	36		
		17	IN31+
IN30-	35		
		16	IN30+
IN29-	34		
		15	IN29+
IN28-	33		
		14	IN28+
IN27-	32		
		13	IN27+
IN26-	31		
		12	IN26+
IN25-	30		
		11	IN25+
IN24-	29		
		10	IN24+
IN23-	28		
		9	IN23+
IN22-	27		
		8	IN22+
IN21-	26		
		7	IN21+
IN20-	25		
		6	IN20+
IN19-	24		
		5	IN19+
IN18-	23		
		4	IN18+
IN17-	22		
		3	IN17+
IN16-	21		
		2	IN16+
AGND	20		
		1	AGND

III. PROGRAMMING INFORMATION

The 9723/AI card responds to word read and writes to the thirty-two Analog Input registers. The card also supports word writes and reads to the control and status register, and word reads of the board identifier PROM. The card's memory map is shown below.

TABLE 6

PAS 9737/AI MEMORY MAP

00	FF	V (56)	01
02	FF	M (4D)	03
04	FF	E (45)	05
06	FF	I (49)	07
08	FF	D (44)	09
0A	FF	P (50)	0B
0C	FF	A (41)	0D
0E	FF	S (53)	0F
10	FF	9 (39)	11
12	FF	7 (37)	13
14	FF	2 (32)	15
16	FF	3 (33)	17
18	FF	A (41)	19
1A	FF	I (49)	1B
1C	FF	A (41)	1D
1E	FF	0 (30)	1F
20	Reserved	Control / Status Reg.	21
22	Reserved	Reserved	23
24	Reserved	Reserved	25
26	Reserved	Reserved	27
28	Reserved	Reserved	29
2A	Reserved	Reserved	2B
2C	Reserved	Reserved	2D
2E	Reserved	Reserved	2F
30	Reserved	Reserved	31
3E	Reserved	Reserved	3F
40	CH 0	CH 0	41
42	CH 1	CH 1	43
	Through	Through	
7C	CH 30	CH 30	7D
7E	CH 31	CH 31	7F

Board IDentifier PROM

The board IDentifier PROM is located at an offset of 00 (hex) from the base address, and can be read with word reads. The least significant byte of the word will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM will handshake, but not transfer any data.

VME Trigger Register

The VME Trigger Register is located at the board’s base address plus E. Writing to this location causes the card to initiate a scan sequence.

Control and Status Register

The Control and Status Register (CSR) is located at the cards base address plus 20, (hex). The word format of the Control and Status Register is shown below.

TABLE 7

Control and Status Register

15-8	7	6	5	4	3	2	1	0
Not Used	Loop Back HT	Loop Back HT	Loop Back HT	Loop Back HT	Loop Back HT	Loop Back HT	Loop Back HT	Loop Back HT

LT = Low True
HT = High True

The CSR is reserved for future use. The only function it currently performs is to echo the data that was written to it. The power up or reset condition of the Control and Status Register is FF00.

The thirty-two Analog Input Channels can be read starting at the board's base address plus 40 (hex). Each register presents the data from one input channel as left justified 12 bit data in a 16 bit field. The unused, (low), four bits are always zero. Data is presented in offset binary.

The table below shows the offset binary codes for several examples of each of the four possible input voltage ranges.

TABLE 8

Offset Binary Codes

+/- 10 V Range	+/- 5 V Range	+ 10 V Range	+ 5 V Range	Offset Binary Data	
Voltage In	Voltage In	Voltage In	Voltage In	Hex	Binary
+10.235	+5.1175	+10.2375	+5.11875	FFF0	1111111111110000
+10.000	+5.000	+10.120	+5.060	FD00	1111110100000000
+0.005	+0.0025	+5.1225	+2.56125	8010	1000000000010000
0.000	0.000	+5.120	+2.560	8000	1000000000000000
-0.005	-0.0025	+5.1175	+2.55875	7FF0	0111111111110000
-10.000	-5.000	+0.1200	+0.060	0300	0000001100000000
-10.240	-5.120	0.000	0.000	0000	0000000000000000

VI. CALIBRATION PROCEDURE

Set the switches and jumper on the card to the shipping position. This sets the address to C000 in short space, +/-10.24 volt inputs and software trigger. Install the 9723/AI card in a VME chassis, and allow the card to stabilize for approximately 1 minute.

Monitor TP5 with a voltmeter and adjust R41 for –5.000V.

Use the test program to scan and display all the inputs.

Connect the voltage standard to Channel 16, input 0.000V and adjust R46 for a reading of 8000.

Input 10.230 volts into channel 16 and adjust R50 for a reading of FFE0.

Input –10.230 volts into channel 16 and verify a reading of 0020.

Repeat any adjustments as required.

Input +10.230V, 0.000V and –10.230V into every channel and verify the readings.

Set up a pulse generator to output a 50% duty cycle 2KHz TTL level pulse.

Close switch SW4-5, and the card should stop scanning. The yellow scan LED will go out, and the data will stop changing slightly. Connect the pulse generator to the card, and observe that it starts scanning again. Remove the pulse generator connection and open SW4-5 and the card will resume scanning.

This completes the calibration procedure.