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PAS 9737/AI-SMT
ENGINEERING SPECIFICATION

64 CHANNEL, 16 BIT
VME ANALOG INPUT CARD
PCB Revision D (07/30/08)

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64 Channel 16 Bit
VME Analog Input Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9737/AI-SMT provides 64 analog input channels multiplexed into a scanning 16-bit Analog to Digital Converter, (ADC). Low pass filters are provided for the analog input signals and four different cutoff frequencies are available as options.

The card is available with a Programmable Gain Amplifier (PGA) with gains of 1 to 128 in eight binary steps. Input voltage ranges of 0 to 10.24V and ± 10.24 Volts at a gain of 1 are available as order options. At a gain of 128 this translates into 0 to 80 mV or ± 80mV ranges. Another version of this card is available with out the PGA and an input voltage range of +/- 10.00 Volts

Input signals enter the card through a pair of 64-pin shrouded headers, that can be used with mass termination ribbon cable. These connectors are located at the card's front panel.

Two 25uA current sources are provided to drive external resistive transducers, such as thermistors and RTDs. These signals are available in a 12-pin connector located between the two analog input connectors.

Two scan rates are available as orderable options. The card can scan at either 100K SPS or 12.5K SPS. Reducing the scan rate to 12.5K SPS provides better accuracy at higher gains. This version of the card is better at measuring low level signals, and uses lower noise amplifiers that require a longer settling time. The 100 KHz card uses higher speed FET amplifiers in the front end, in order to settle in less than 10 microseconds. The ordering options are defined by dash numbers, which are described in the ordering information section of this specification.

Digitized analog data is available to the VME bus through a dual ported RAM interface that can be read while the card continues scanning. Thirty-two bit data reads are supported, which allows two converted values to be read with a single VME transfer. VME systems with A16, A24, or A32 addressing are supported, which allows the card's base address to be located anywhere in the VME address range.

Additional features include a board identifier registers, control and status register, and scan configuration registers.

Card Features: PAS 9737/AI-SMT

- 64 differential analog input channels
- Differential or single ended inputs jumper configurable per channel
- Optional low pass filters with corner frequencies of 10 Hz, 50 Hz, 100 Hz or 500 Hz
- Analog inputs on two ea. 64-position connectors, allows the use of mass termination cable.
- 16 bit 100 KHz Analog to Digital Converter (ADC)
- Constantly scans selected channels and stores digitized results in dual port memory
- Programmable Gain Amplifier (PGA) with gains of 1 to 128 (optional)
- Input range of +/- 10.00 Volts, +/- 10.24 Volts or 0 to 10.24 Volts (optional)
- Two 25 uA current sources provided for transducer excitation
- Over voltage protected inputs with power on or off
- VME 6U form factor; 233 mm x 160 mm card size
- VME access: D32,D16; A32, A24, A16 Slave
- Optional VME SYSFAIL asserts on power up, jumper selectable
- Three LED's provided on the front panel; Pass, Fail, and Board Access LED's
- Board Identifier registers. (Board ID is VMEIDPAS9737AIC0 or C1)
- Analog section is powered by +/- 15 Volts DC to DC converter
- Operating temperature range 0 to 60 deg. C.

II. SPECIFICATIONS

Electrical Specifications
(Un-filtered Cards)

Number of Channels	64 differential or single ended inputs
Analog Input Range At G = 1	Bipolar +/-10.00 or +/- 10.24 Volts Unipolar 0.000 to + 10.240
Programmable Gains	1,2,4,8,16,32,64,128
Resolution	16 bits
Accuracy	+/-(0.005% of reading + 0.005% FSR +100 uV)
Temperature stability	+/-(10 PPM of reading + 7.5 PPM of FSR + 2.5 uV)/deg. C
Input bias current	40 nAmps (max.) at 0.0 Volts input
Input Impedance	5 M Ohm in parallel with 50 pF
CH.-to-CH. crosstalk	90 dB
Common mode voltage	+/- 11 Volts signal plus common mode
Common mode rejection (DC to 60 Hz, 350-ohm imbalance)	Gain =1 90 dB (min.),100 dB (typ.)
Over voltage protection	+/- 35 VDC sustained, power on or off
Card Power Requirements	5 Volts @ 1 Amp, (typ.)

Low Pass Filter Options*

0 = No filter
1 = 10 Hz filter
2 = 50 Hz filter
3 = 100 Hz filter
4 = 500 Hz filter

*Note: Low pass filters are specified at the approximate frequency where the input voltage is attenuated by 6 dB as defined by the following expression; 20 log V(out) / V(in). The leakage impedance of the capacitors used in the input filters forms a voltage divider with the input resistors, which results in slight variations in the gain from channel to channel. This effect is most pronounced on the 10 Hz version of the filters because they use the highest value of capacitance, thus have the highest leakage current.

Environmental Specifications

Operating Temperature Range	0 to 60 degrees C.
Storage Temperature Range	-20 to 85 degrees C.
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Dbl (160 mm x 233 mm)
Weight	12 oz. (typ.)
Connectors	2 ea. 96 position, (VME bus connectors) 2 ea. 64 position, (Analog Input) 1 ea. 12 pin shrouded header (external sync.in, out & current sources)

Ordering Information

The 9737/AI-SMT card is available in several different configurations that are defined by dash numbers. Each dash number has three digits defined as XYZ. Each digit defines a certain feature of the card, in this case the filter type, scan rate, and input voltage range. The various dash numbers are defined below.

XYZ Definitions

0YZ = 0 100K Hz scan rate
1YZ = Low voltage measurement version, 12.5 KHz

X**0**Z = No Input Filter
X**1**Z = 10 Hz Low Pass Input Filter
X**2**Z = 50 Hz Low Pass Input Filter
X**3**Z = 100 Hz Low Pass Input Filter
X**4**Z = 500 Hz Low Pass Input Filter

XY**0** = +/- 10.00 Volt Full Scale Input Range, no PGA*
XY**1** = +/- 10.24 Volt Full Scale Input Range, with PGA*
XY**2** = 0 to +10.24 Volt Full Scale Range, with PGA*

*PGA = Programmable Gain Amplifier

EXAMPLE: A dash number of 121 would specify a card with 50 Hz Low Pass Input Filters, a +/- 10.24 Volt Full Scale Input Range with a PGA, and the card is optimized for low voltage measurements. When ordering, the dash number follows the model number = ***PAS 9737/AI-121***.

Switches and Jumper Plug Definitions

The PAS 9737/AI-SMT card contains two eight-position DIP switches, two three-position DIP switch, and sixty five jumper plugs. DIP switches one through three are used to set the card's VME address and are defined in Table 1 below. When a switch is closed or on, the corresponding address bit must be low to select the card's address, and when a switch is open or off, the corresponding address bit must be high.

Switches SW4-1 and 2 are used to select the card's operating environment; A16, A24, or A32. The setting of these switches is defined in Table 2 on page 11. SW4-3 currently has no function.

Jumper plug 2 controls the SYSFAIL line as described in the table 1.

TABLE 1

SWITCH AND JUMPER DEFINITIONS

Switch #	Function
SW1-1	A13
SW1-2	A14
SW1-3	A15
SW2-1	A16
SW2-2	A17
SW2-3	A18
SW2-4	A19
SW2-5	A20
SW2-6	A21
SW2-7	A22
SW2-8	A23
SW3-1	A24
SW3-2	A25
SW3-3	A26
SW3-4	A27
SW3-5	A28
SW3-6	A29
SW3-7	A30
SW3-8	A31
J2 IN	SYSFAIL controlled by control register

TABLE 2

SWTICH DEFINITIONS

SW4-1	SW4-2	Address Modifiers	Address Space
Closed	Closed	09, 0D	Extended
Open	Closed	39, 3D	Standard
Closed	Open	29, 2D	Geographical *
Open	Open	29, 2D	Short

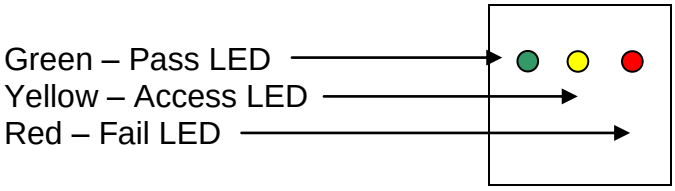
*Requires a special chassis

Jumpers JP0 through JP63 are used to connect the low side of each channel to a common trace on the PCB and are available as an option. Normally the input signal wiring will take advantage of the card's differential inputs, and run separate wires from the high and low sides of the inputs back to the input signal sources. In cases where all or some of the inputs are referenced to a common ground, the jumpers can be installed to tie the low sides of the input channels together, and a single ground wire can be run to the common ground point. Any unused inputs need to connect to high and low sides of the channel together, and ideally tie them to ground.

Front Panel LED Definitions

Three LED's are available at the front panel to indicate the board's status. The position of the LEDs is shown below.

Top of Front Panel



The Fail LED powers up on, and is controlled with bit 0 of the control register. Writing a one to bit 0 will turn off this LED. The state of this LED is reflected in bit 0 of the status register. When the Fail LED is on, and J2 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the control register. This LED will be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the status register reflects the state of this LED. Once the board has passed some initial power up tests this LED can be turned on to indicate successful completion of the power up sequence. The yellow access LED will turn on anytime the board is accessed.

Connector Definitions

Two 96-position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. A pair of 64 position, shrouded headers are installed through the board's front panel to provide access to the sixty-four analog input channels

All unused input channels should be shorted from high to low and ideally have both sides connected to ground.

A twelve position shrouded header is provided between the 64 position connectors to provide access to the board's two, 25 micro Amp current sources. Pins are also provided in this connector for external synchronization input and output signals, however these functions have not been implemented in this revision of the board. The pin definitions of these connectors are provided below and on the following pages.

TABLE 3

12 Position Shrouded Header, P5

Signal Name	Pin#		Signal Name
Analog Ground	12	11	Ground
Current Source 2	10	9	External Sync Out (RFU)
Analog Ground	8	7	Ground
Analog Ground	6	5	External Sync In (RFU)
Current Source 1	4	3	Ground
Analog Ground	2	1	External Clock In (RFU)

RFU= Reserved for Future Use

Pins 1 and 2 are the lowest pins in the connector when the board is installed vertically in a VME chassis. Pin 2 is located next to the PCB and pin 1 is located directly behind it. This applies to the 64 position connectors, P3 and P4, and the 12 position connector P5.

TABLE 4

Analog Input Connector P3

64 Pin Top Connector

Pin Numbers			
CH63H	64	63	CH63L
CH62H	62	61	CH62L
CH61H	60	59	CH61L
CH60H	58	57	CH60L
CH59H	56	55	CH59L
CH58H	54	53	CH58L
CH57H	52	51	CH57L
CH56H	50	49	CH56L
CH55H	48	47	CH55L
CH54H	46	45	CH54L
CH53H	44	43	CH53L
CH52H	42	41	CH52L
CH51H	40	39	CH51L
CH50H	38	37	CH50L
CH49H	36	35	CH49L
CH48H	34	33	CH48L
CH47H	32	31	CH47L
CH46H	30	29	CH46L
CH45H	28	27	CH45L
CH44H	26	25	CH44L
CH43H	24	23	CH43L
CH42H	22	21	CH42L
CH41H	20	19	CH41L
CH40H	18	17	CH40L
CH39H	16	15	CH39L
CH38H	14	13	CH38L
CH37H	12	11	CH37L
CH36H	10	9	CH36L
CH35H	8	7	CH35L
CH34H	6	5	CH34L
CH33H	4	2	CH33L
CH32H	2	1	CH32L

Terminate all unused input channels.

TABLE 5

Analog Input Connector P4

64 Pin Bottom Connector

Pin Numbers			
CH31H	64	63	CH31L
CH30H	62	61	CH30L
CH29H	60	59	CH29L
CH28H	58	57	CH28L
CH27H	56	55	CH27L
CH26H	54	53	CH26L
CH25H	52	51	CH25L
CH24H	50	49	CH24L
CH23H	48	47	CH23L
CH22H	46	45	CH22L
CH21H	44	43	CH21L
CH20H	42	41	CH20L
CH19H	40	39	CH19L
CH18H	38	37	CH18L
CH17H	36	35	CH17L
CH16H	34	33	CH16L
CH15H	32	31	CH15L
CH14H	30	29	CH14L
CH13H	28	27	CH13L
CH12H	26	25	CH12L
CH11H	24	23	CH11L
CH10H	22	21	CH10L
CH9H	20	19	CH9L
CH8H	18	17	CH8L
CH7H	16	15	CH7L
CH6H	14	13	CH6L
CH5H	12	11	CH5L
CH4H	10	9	CH4L
CH3H	8	7	CH3L
CH2H	6	5	CH2L
CH1H	4	3	CH1L
CH0H	2	1	CH0L

Terminate all unused input channels.

III. PROGRAMMING INFORMATION

The 9737/AI-SMT card responds to word and longword reads of the sixty-four analog input channels, and the thirty two bit test register. The card also supports word writes and reads to the control and status register, and the various scan registers, and word reads of the board identifier registers. The card's memory map is shown below.

TABLE 6

PAS 9737/AI MEMORY MAP

BASE +0000	00	V (56)	BASE +0001
0002	00	M (4D)	0003
0004	00	E (45)	0005
0006	00	I (49)	0007
0008	00	D (44)	0009
000A	00	P (50)	000B
000C	00	A (41)	000D
000E	00	S (53)	000F
0010	00	9 (39)	0011
0012	00	7 (37)	0013
0014	00	3 (33)	0015
0016	00	7 (37)	0017
0018	00	A (41)	0019
001A	00	I (49)	001B
001C	00	C (43)	001D
001E	00	1 (31)	001F
0020	97	37	0021
Thru	Reserved	Reserved	Thru
003E	Reserved	Reserved	003F
0040	Reserved	Control & Status	0041
0042	Reserved	ADC Scan Mode	0043
0044	Reserved	Reserved	0045
Thru	Reserved	Reserved	Thru
007E	Reserved	Reserved	007F
0080	CH 0	Gain	0081
Thru	CH X	Gain	Thru
00FE	CH 63	Gain	00FF
0100	Channel 0 Data		0101
0102	Channel 1 Data		0103
0104	Channel 2 Data		0105
0106	Channel 3 Data		0107
0108	Channel 4 Data		0109
010A	Channel 5 Data		010B
010C	Channel 6 Data		010D
010E	Channel 7 Data		010F
1FFE	Last Channel Data		1FFF

Board Identifier PROM (Base Address + 000H to 01FH) Read Only

The Board Identifier registers are located starting at the board's base address plus 1, and continues to the base address plus 1F.

Byte and word reads to the Identifier registers are supported. Only the least significant byte of a word read will contain valid data, and the most significant byte will contain 00. The ID registers contain 16 ASCII characters that specify the board's model number and revision level. The 100 KHz version of the card will return revision C1. The 12.5 KHz version of the card will return revision C0. A write to the ID register locations will handshake, but not transfer any data.

Fast ID Register (Base Address + 20H) Read Only

The fast ID register is located at the card's base address plus 20. Reads to this register will return the hex value 9737, which is the board's model number. Writing to this register will handshake, but not transfer any data.

Control and Status Register (Base Address + 40H) Read/Write

TABLE 7

Control and Status Register

16-5			4	3	2	1	0
Loop Back	Loop Back	Loop Back	SW Reset Pulse	Loop Back	ADC Stop	Pass LED	Fail LED

Bits 16-5 Loopback. These bits will return the values last written to them.

Bit 4 Writing a 1 to this bit will generate a software-reset pulse. The software reset stops the conversion in process. It also resets the scan mode register, and disables scanning. This bit will always return a 0 when read.

Bit 3 Loopback. This bit will return the value that was last written to it.

Bit 2 This bit indicates that a conversion has not occurred in the last 10 mSec. Writing this bit has no effect.

1 = ADC has not performed a conversion in the last 10 mSec.
0 = ADC has performed a conversion in the last 10 mSec

Bit 1 This bit controls the Pass LED

1 = Turn on the Pass LED
0 = Turn off the Pass LED

Bit 0 This bit controls the Fail LED. The SYSFAIL line will also be asserted when the Fail LED is on.

1 = Turn off the Fail LED
0 = Turn on the Fail LED

ADC Scan Mode Register (base + 42)

This 8-bit register determines the scanning mode for the analog inputs used on this board. The bits are defined below:

TABLE 8

ADC Scan Mode Register

15	14	13	12	11	10	9	8
Loop Back	Loop Back	Loop Back	Loop Back	Loop Back	Loop Back	Loop Back	Loop Back
7	6	5	4	3	2	1	0
Enable Scan	Continue Scan	Gain Init	Loop Back	Loop Back	Scan Mode 2	Scan Mode 1	Scan Mode 0

Bit 15 through 8 are loop-back bits and will return the value last written to them.

Bit 7 This bit is used to enable or disable scanning of the analog input channels. The enable scan bit is cleared on power up, SYSRST or software reset.

When the enable scan bit is set, and the continuous scan bit is also set, the card will continue scanning until scanning is disabled, either with a write to the scan mode register or with a reset.

When the enable scan bit is set and the continuous scan bit is not set, the card will perform one scan of the specified number of channels, and then stop. Once the scan is complete, the enable scan bit will reset to a zero. A new scan can be initiated by writing to the scan mode register with the enable scan bit set.

0 = Scanning Disabled
1 = Scanning Enabled

Bit 6 This bit enables or disables continuous scanning of the analog input channels. When continuous scanning is enabled the scan sequencer will start the scan sequence over once the last channel has been sampled. The continuous scan bit is cleared on power up, SYSRST or software reset.

0 = Continuous scanning disabled
1 = Continuous scanning enabled

Bit 5 This bit is used to enable the sequencer to use channel gain values that are stored in memory. When the gain initialized bit is clear the sequencer will scan all of the channels at unity gain. The gain-initialized bit is cleared on power up, SYSRST or software reset. This bit is only functional on cards with the PGA option (XY1 or XYZ).

0 = Sample all channels at unity gain
1 = Sample each channel at the gain specified by the Channel Gain Memory

Bits 4-3 Loopback. These bits will return the last value written to them.

Bits 2-0 These bits are used to determine how many times the sequencer will scan the sixty-four input channels before it either stops or repeats the scan. The bits are defined in Table 9.

TABLE 9

Scan Mode Bits 2 - 0

SM2	SM1	SM0	Blocks Scanned	Stop Address
0	0	0	1	017F
0	0	1	1	017F
0	1	0	2	01FF
0	1	1	4	02FF
1	0	0	8	04FF
1	0	1	16	08FF
1	1	0	32	10FF
1	1	1	62	1FFF

TABLE 10

Channel Gain Memory (base + 80 - FF)

7	6	5	4	3	2	1	0
					Gain 2	Gain 1	Gain 0

The Channel Gain Memory is used to specify the gain that each channel will use when sampling and converting input signals. This information must be programmed before the card begins sampling data. Memory location 81 contains the gain for channel 0 and the gain information for subsequent channels is contained in the ascending odd memory locations. The gain value for channel 63 is contained at location FF. Gain can be programmed in binary steps from 1 to 128, and the gain codes are shown below. The gain values can be read back over the VME bus when the card is not scanning input channels. When the card is scanning the gain values are only available to the scan sequencer. The gain memory is only available on cards with the PGA option (XY1 and XYZ).

TABLE 11

Gain Codes

Gain 2	Gain 1	Gain 0	Gain Value	Full Scale Range	Unipolar Full Scale Range
0	0	0	1	+/- 10.24 V	0 to 10.24 V
0	0	1	2	+/- 5.12 V	0 to 5.12 V
0	1	0	4	+/- 2.56 V	0 to 2.56 V
0	1	1	8	+/- 1.28 V	0 to 1.28 V
1	0	0	16	+/- 640 mV	0 to 640 mV
1	0	1	32	+/- 320 mV	0 to 320 mV
1	1	0	64	+/- 160 mV	0 to 160 mV
1	1	1	128	+/- 80 mV	0 to 80 mV

Channel Data Memory (100 – 1FFF)

The Channel Data Memory is used to store the converted values form the scanned channels. Data is stored in 16 bit, 2's complement format. The first value in a data scan will be stored at location 100 and the sequencer can fill the entire RAM array up to address 1FFF. When scanning is disabled, the VME bus can write to the Channel Data Memory. This allows the memory to be filled with test patterns and then read back to verify the functionality of the memory and the data busses. When the card is scanning, writes from the VME bus are disabled, and only the scan sequencer can write to the Channel Data Memory.

The card can be programmed to use as little as 64 words of Channel Data Memory, or up to 3968 words. When the card is programmed to fill blocks of data with 64 channels per block, the second block will start at location 180(hex).

Once a scan is complete, the card can be programmed to automatically start the scan over, or to stop the scan sequencer. A convenient way to use this card is to set the card to scan all of the channels, and then repeat the scan cycle. Whenever a data value is required, the program can read the desired memory location and get the latest digitized analog value. In this mode of operation, the card's response time similar to a digital input card.

IV. CALIBRATION PROCEDURE for +/- 10.24V Card with PGA

Install the PAS 9737/AI-SMT card in a VME chassis, and allow the card to stabilize for approximately five minutes. A test program is required that will read and display the values of all channels on the card.

ADC Zero Adjustment (R61)

Connect a precision voltage standard to the input of channel zero, with the high side of the voltage standard connected to the low side of the channel, (P4I-1) and the low side of the voltage standard connected to the high side of the channel, (P4I-2). Connect the low side of the channel to earth ground, and select 0.0000 Volts out of the voltage standard. Adjust R61 for a reading of 0000 (hex) on channel zero.

ADC Gain Adjustment (R44)

Leave the voltage standard configured as in the previous step, and select –10.2375 Volts out of the standard. Adjust R44 for a reading of 7FF8 (hex). Select +10.2375 Volts out of the voltage standard, and verify a reading of 8008 (hex).

Common Mode Adjustment (R37)

Reverse the leads from the voltage standard to the card. The high side of the voltage standard is connected to the high side of the channel (P4I-2), and the low side of the voltage standard is connected to the low side of the channel (P4I-1). Select +10.2375 Volts out of the standard and adjust R37 for a reading of 7FF8 (hex). Select –10.2375 Volts out of the standard, and verify a reading of 8008 (hex).

PGA Zero Adjustment (R38)

Set up the test program to scan all of the even channels at a gain of one, and all of the odd channels at a gain of 32. Short the inputs of all channels together, and connect all inputs to the card's analog ground. Adjust R38 so that all channels display the same digital value. Adjust R61 until all channels read zero counts. Verify all previous calibrations, and repeat any adjustments as necessary.

All Inputs Functional Test

Set up the test program to scan all channels at a gain of one. Input +10.2375 Volts, 0.0000 Volts and –10.2375 Volts on each channel, one channel at a time, and verify the proper digital value.

Current Source Adjustment

Refer to Section V.

V. CALIBRATION PROCEEDURE for +/- 10.000V Card without PGA

Install the PAS 9737/AI-SMT card in a VME chassis, and allow the card to stabilize for approximately five minutes. A test program is required that will read and display the values of all channels on the card.

ADC Zero Adjustment (R61)

Connect a precision voltage standard to the input of channel zero, with the high side of the voltage standard connected to the low side of the channel, (P4I-1) and the low side of the voltage standard connected to the high side of the channel, (P4I-2). Connect the low side of the channel to earth ground, and select 0.0000 Volts out of the voltage standard. Adjust R61 for a reading of 0000 (hex) on channel zero.

ADC Gain Adjustment (R44)

Leave the voltage standard configured as in the previous step, and select –9.9976 Volts out of the standard. Adjust R44 for a reading of 7FF8 (hex). Select +9.9976 Volts out of the voltage standard, and verify a reading of 8008 (hex).

Common Mode Adjustment (R37)

Reverse the leads from the voltage standard to the card. The high side of the voltage standard is connected to the high side of the channel (P4I-2), and the low side of the voltage standard is connected to the low side of the channel (P4I-1). Select +9.9976 Volts out of the standard and adjust R37 for a reading of 7FF8 (hex). Select –9.9976 Volts out of the standard, and verify a reading of 8008 (hex).

All Inputs Functional Test

Set up the test program to scan all channels at a gain of one. Input +9.9976 Volts, 0.0000 Volts and –9.9976 Volts on each channel, one channel at a time, and verify the proper digital value.

Current Source Adjustment

Connect an amp-meter between pins 2 and 4 of P5 and adjust R63 for a reading of 25.0 micro-Amps. Connect the amp-meter between pins 10 and 12 of P5 and adjust R67 for a reading of 25.0 micro-Amps.