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PAS 9764/DI
ENGINEERING SPECIFICATION

32 BIT CHANGE OF STATE w/ TIME STAMPING
VME DIGITAL INPUT CARD
PCB Revision B (4/18/2002)

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32 Bit Change of State w/ Time Stamping
VME Digital Input Card

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32 Bit Change of State Card w/ Time Stamping VME Digital Input Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9764/DI is a VME based, 32 channel, digital input card with Change of State (COS) detection and time stamping. Input signals are monitored and when a change of state is detected, the card stores the state of the input signals and the time of the change, as determined by an internal clock, in an on board FIFO memory. The FIFO can be read from the VME bus to retrieve the input state and time data. VME interrupts will be generated in the event of transitions on selected input signals.

This card can be used in VME systems with A16, A24, or A32 addressing, and data bus widths of 16 and 32 bits are supported. Jumper plugs are used to configure the width of the address bus. VME instruction types determine the width of the data bus. The input signals are connected to a pair of 50 position shrouded headers mounted through the front panel. A board identifier PROM, interrupt vector register, and control register are provided in addition to the 32 bit counter and 64K word by 32 bit FIFO.

Card Features: PAS 9764/DI

- Differential input bits with characteristics specified by EIA-422B
- A version of the card with TTL compatible inputs is available as an option
- Input signals on two 50 position shrouded headers at the front panel
- Detects change of state on low to high transition or high to low transition
- Time stamps every transition and stores data and time stamp in a FIFO memory. The FIFO is 32 bits wide by 64K words deep
- VME interrupts are generated if the line that changed was enabled to generate interrupts
- VME bus reads 32 bits of data followed by 32 bits of time from the FIFO
- Counters are enabled with a control word write
- Status register contains the following bits; Pass, Fail, Monitor Enable, Interrupt Enable, Interrupt Level, Counter Rate, FIFO Empty, FIFO Half Full, FIFO Full
- VME 6U form factor; 233 mm x 160 mm card size
- VME access: D32, D16; A32, A24, A16 Slave. VME Interrupter
- Optional VME SYSFAIL assert on power up
- Four status LED’s on the front panel consisting of, Pass, Fail, Monitoring Enabled and FIFO Full.
- Board Identifier PROM; ID code is VMEID PAS9764DI ** (** is the revision level)

II. SPECIFICATIONS

Electrical Specifications

Number of Channels	32
Card Power Requirements	5 Volts @ 2 Amps (typ)

EIA-422B Differential Inputs

Positive going threshold	200 mV (max.)
Negative going threshold	- 200 mV (min.)
Hysteresis	120 mV (typ.)
Input Resistance (Termination Resistors Removed)	12 K Ohm (min.) 18 K Ohm (typ.)
Input Resistance (Termination Resistors Installed)	100 Ohm (typ.)

TTL Compatible Inputs

Low level input voltage	0.8V (max)
High level input voltage	2.0V (min)
Input leakage current	+/-10uA (max)

Ordering Information

When ordering the differential input version of the card, specify model number *PAS 9764/DI*. When ordering the TTL input version of the card, specify model number *PAS 9764/DI-TTL*.

Environmental Specifications

Operating Temperature Range	0 to 60 degrees Celsius with forced air cooling.
Storage Temperature Range	-20 to 85 degrees C.
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	16 oz. (typ)
Connectors	2 ea. 96 pos. DIN (VME bus connectors) 2 ea. 50 pin header (input data connector) 3M # 3433-5602

Jumpers and Indicators

The 9764/DI card contains 27 jumper plugs and four LED indicators. Twenty four jumpers are used to set the board's VME base address, and are defined in table 1 on page 8. When a jumper is installed, the corresponding address bit must be low to select the card's address. When a jumper is removed the corresponding address bit must be high. The card is shipped configured for address F0000000, so that 20 of the possible 24 address jumpers are installed. J8-J27 are installed, J28-J31 are removed.

Jumpers J1 and J2 are used to select the boards operating environment, either A16, A24 or A32, and the installation of these jumpers is defined in table 1. J1 and J2 are installed for shipment, to select 32 bit addressing.

Jumper J4 allows the SYSFAIL line to be driven with bit 0 of the control register when it is installed. The card is shipped with J4 installed.

TABLE 1

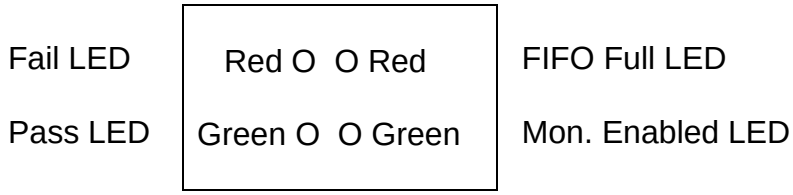
PLUGGABLE JUMPER DEFINITIONS

Jumper #	Function
J1 IN, J2 IN	A32 Addressing
J1 IN, J2 OUT	A24 Addressing
J1 OUT, J2 X	A16 Addressing
J4 IN	SYSFAIL steered by control register
J8	A8
J9	A9
J10	A10
J11	A11
J12	A12
J13	A13
J14	A14
J15	A15
J16	A16
J17	A17
J18	A18
J19	A19
J20	A20
J21	A21
J22	A22
J23	A23
J24	A24
J25	A25
J26	A26
J27	A27
J28	A28
J29	A29
J30	A30
J31	A31

Front Panel LED's

Four LED's arranged in a 2 by 2 array are provided at the front panel to indicate the board's status. The position of the LED's is shown below

Top of Front Panel



The Fail LED powers up on, and is controlled with bit 0 of the control register. This LED can be turned off by writing a one to bit 0. The state of this LED is reflected in bit 0 of the status register. When the Fail LED is on, and J4 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the control register. This LED can be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the status register reflects the state of this LED. Once the board has passed some initial power up tests this LED can turned on to indicate successful completion of the power up sequence.

The FIFO Full LED indicates that the on board FIFO is full. The status of this LED is reflected in bit fifteen of the status register.

The Monitor Enabled LED will turn when the board is enabled to detect changes. The state of this LED is reflected in bit two of the status register.

Connector Definitions

Two 96 position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. Two 50 position shrouded headers are installed through the board's front panel to provide access to the thirty-two input channels. The pin out of the input connectors is defined below and on the following page.

TABLE 2

P3 Connector Pin Definitions

P3 Top Connector

GND	50	49	GND
GND	48	47	GND
N/C	46	45	N/C*
N/C	44	43	N/C*
N/C	42	41	N/C*
N/C	40	39	N/C*
N/C	38	37	N/C*
N/C	36	35	N/C*
N/C	34	33	N/C*
CH0HI	32	31	CH0LO*
CH1HI	30	29	CH1LO*
CH2HI	28	27	CH2LO*
CH3HI	26	25	CH3LO*
CH4HI	24	23	CH4LO*
CH5HI	22	21	CH5LO*
CH6HI	20	19	CH6LO*
CH7HI	18	17	CH7LO*
CH8HI	16	15	CH8LO*
CH9HI	14	13	CH9LO*
CH10HI	12	11	CH10LO*
CH11HI	10	9	CH11LO*
CH12HI	8	7	CH12LO*
CH13HI	6	5	CH13LO*
CH14HI	4	3	CH14LO*
CH15HI	2	1	CH15LO*

*These inputs are grounded on the TTL version of the card.

TABLE 3

P4 Connector Pin Definitions

P4 Bottom Connector

GND	50	49	GND
GND	48	47	GND
CLOCK	46	45	GND
N/C	44	43	N/C*
N/C	42	41	N/C*
N/C	40	39	N/C*
N/C	38	37	N/C*
N/C	36	35	N/C*
N/C	34	33	N/C*
CH16HI	32	31	CH16LO*
CH17HI	30	29	CH17LO*
CH18HI	28	27	CH18LO*
CH19HI	26	25	CH19LO*
CH20HI	24	23	CH20LO*
CH21HI	22	21	CH21LO*
CH22HI	20	19	CH22LO*
CH23HI	18	17	CH23LO*
CH24HI	16	15	CH24LO*
CH25HI	14	13	CH25LO*
CH26HI	12	11	CH26LO*
CH27HI	10	9	CH27LO*
CH28HI	8	7	CH28LO*
CH29HI	6	5	CH29LO*
CH30HI	4	3	CH30LO*
CH31HI	2	1	CH31LO*

* These inputs are grounded on the TTL version of the card.

III. PROGRAMMING INFORMATION

The 9764/DI card responds to word and longword transfers to the, 32 bit Time Counter Register, Interrupt Enable Register, Change Enable Register and FIFO. Word reads of the board identifier PROM, Control and Status Register, FIFO Counter Register and Interrupt Vector Register are also supported. The card's memory map is shown below.

TABLE 4

PAS 9764/DI MEMORY MAP

BASE + 00	ID PROM	V (56)	01
02	(FF)	M (4D)	03
04	(FF)	E (45)	05
06	(FF)	I (49)	07
08	(FF)	D (44)	09
0A	(FF)	P (50)	0B
0C	(FF)	A (41)	0D
0E	(FF)	S (53)	0F
10	(FF)	9 (39)	11
12	(FF)	7 (37)	13
14	(FF)	6 (36)	15
16	(FF)	4 (34)	17
18	(FF)	D (44)	19
1A	(FF)	I (49)	1B
1C	(FF)	A (41)	1D
1E	IDPROM	0 (30)	1F
20	Reserved	Reserved	21
7E	Reserved	Reserved	7F
80	Control/Status	Control/Status	81
82	FIFO Counter	FIFO Counter	83
84	Reserved	Int Vector	85
86	Reserved	Reserved	87
8E	Reserved	Reserved	8F
90	Time Cnt MS	Time Cnt MS	91
92	Time Cnt LS	Time Cnt LS	93
94	Int Enbl MS	Int Enbl MS	95
96	Int Enbl LS	Int Enbl LS	97
98	Chg Enbl MS	Chg En MS	99
9A	Chg Enbl LS	Chg Enbl LS	9B
9C	FIFO MS	FIFO MS	9D
9E	FIFO LS	FIFO LS	9F
A0	Reserved	Reserved	A1
FE	Reserved	Reserved	FF

Board Identifier PROM (Base + 00 hex)

The Board Identifier PROM is located at an offset of 00 (hex) from the base address, and can be read with word reads only. The least significant byte of the word will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM will handshake, but not transfer any data.

Control and Status Register (Base + 80 hex)

The Control and Status Register (CSR) is located at the board's base address plus 80 (hex), and can be written and read with word transfers. The CSR is used to check the FIFO status, control the interrupt level and logic, set the clock frequency, reset the card, and control the front panel LED's. The word format for the Control and Status Register is shown below in Table 5.

TABLE 5

Control and Status Register

15	14	13	12	11	10	9	8
FIFO Full	FIFO Half	FIFO Emty	Loop Back	Loop Back	Int. Clear	Rate 1	Rate 0

7	6	5	4	3	2	1	0
Int. Level	Int. Level	Int. Level	SW Reset Pulse	Int. Enbl.	Mon. Enbl.	Pass LED	Fail LED

Bits 15-13 FIFO Status. These bits are used to read the status of the FIFO memory. They are high true and report how much data is in the FIFO. Writing these bits has no effect on the card.

Bits 12-11 Loopback. These bits will return the value that was last written to them.

Bit 10 Writing a 1 to bit ten clears the interrupt request. This bit will always return a 0 when read.

Bits 9,8 Rate. These bits determine the rate of the on board clock that is used to time stamp the input data. The decoding of these bits is shown below. Reading these bits will return the value that was last written.

Bit 9	Bit 8	Clock Period	Clock Frequency
0	0	1 uSec.	1 MHz
0	1	10 uSec.	100 KHz
1	0	100 uSec	10 KHz
1	1	RFU	RFU

Bits 7-5 Interrupt Level. These bits determine which level VME interrupt will be generated by the board. They return the values last written to them.

Bit 4 Writing a 1 to this bit will generate a software reset pulse. The software reset clears the FIFO Counter Register, Time Counter Register, Interrupt Enable Register, Change Enable Register and clears the FIFO's. This bit will always return a 0 when read.

Bit 3 Interrupt Enable. Writing a one to this bit enables the card to generate VME interrupts. Writing a zero to this bit disables VME interrupts. This bit will return the value that was last written to it.

Bit 2 Monitor Enable. Writing a one to this bit enables the card to monitor the input signals for changes. Writing a zero to this bit disables input monitoring. This bit will return the value that was last written to it.

Bit 1 This bit controls the Pass LED. Reading this bit returns the value that was last written to it.

1 = Turn on the Pass LED
0 = Turn off the Pass LED

Bit 0 This bit controls the Fail LED. The SYSFAIL line will also be asserted when the Fail LED is on if J4 is installed. Reading this bit returns the value that was last written to it.

1 = Turn off the Fail LED
0 = Turn on the Fail LED

FIFO Counter Register (Base + 82 hex)

The FIFO Counter Register is used to read the number of longwords that are in the FIFO. This register is incremented each time the FIFO is written with a new 32 bit word of data or time. It will decrement each time 32 bits are read out of the FIFO. Values 0000 hex to FFFF hex can be read from the FIFO counter. A value of 0000 indicates the FIFO is empty and FFFF indicates that there is one open location. The control and status register contains additional status bits for the FIFO. These are full, half full and empty. The word format for the FIFO Counter Register is shown below in Table 6.

TABLE 6

FIFO Counter Register

15	14	13	12	11-4	3	2	1	0
FIFO Count 15	FIFO Count 14	FIFO Count 13	FIFO Count 12	FIFO Count 11-4	FIFO Count 3	FIFO Count 2	FIFO Count 1	FIFO Count 0

Interrupt Vector Register (Base + 85 hex)

Writing this eight bit register determines the board's interrupt vector. The register can be read back to verify the interrupt vector. The bits in this register are defined below in Table 7.

TABLE 7

Interrupt Vector Register

7	6	5	4	3	2	1	0
Int Vect 7	Int Vect 6	Int Vect 5	Int Vect 4	Int Vect 3	Int Vect 2	Int Vect 1	Int Vect 0

Time Counter Register (Base + 90, 92 hex)

The Time Register is used to read the state of the board's 32 bit clock. Time can be read when the board has input monitoring enabled. When input monitoring is disabled, the time register is held clear. The time register can be read with a 32 bit longword transfer or two 16 bit word transfers. The word format for the Time Counter Register is shown on the next page in Tables 8 & 9.

TABLE 8

Time Counter Most Significant Register (Base + 90 hex)

15	14	13	12	11-4	3	2	1	0
Time MS 31	Time MS 30	Time MS 29	Time MS 28	Time MS 27-20	Time MS 19	Time MS 18	Time MS 17	Time MS 16

TABLE 9

Time Counter Least Significant Register (Base + 92 hex)

15	14	13	12	11-4	3	2	1	0
Time LS 15	Time LS 14	Time LS 13	Time LS 12	Time LS 11-4	Time LS 3	Time LS 2	Time LS 1	Time LS 0

Interrupt Enable Register (Base + 94, 96 hex)

The Interrupt Enable Register is used to define which input bits will generate VME interrupts when they change states. Writing a one to a specific bit location enables interrupt generation for that bit, and a zero disables interrupting. The state of this register can be read back to determine which bits are enabled to generate interrupts. This register can be read or written with a 32 bit longword transfer or two 16 bit word transfers. The word format for the Interrupt Enable Register is shown below in Tables 10 & 11.

TABLE 10

Interrupt Enable Most Significant Register (Base + 94 hex)

15	14	13	12	11-4	3	2	1	0
Int En MS 31	Int En MS 30	Int En MS 29	Int En MS 28	Int En MS 27-20	Int En MS 19	Int En MS 18	Int En MS 17	Int En MS 16

TABLE 11

Interrupt Enable Least Significant Register (Base + 96 hex)

15	14	13	12	11-4	3	2	1	0
Int En LS 15	Int En LS 14	Int En LS 13	Int En LS 12	Int En LS 11-4	Int En LS 3	Int En LS 2	Int En LS 1	Int En LS 0

Change Enable Register (Base + 98, 9A hex)

The Change Enable Register is used to define which input bits will cause the FIFO to be updated when they change states. Writing a one to a specific bit location enables FIFO updates for that bit, and a zero disables updating the FIFO. The state of this register can be read back to determine which bits are enabled to generate changes. This register can be read or written with a 32 bit longword transfer or two 16 bit word transfers. The word format for the Change Enable Register is shown below in Tables 12 & 13.

TABLE 12

Change Enable Most Significant Register (Base + 98 hex)

15	14	13	12	11-4	3	2	1	0
CEN MS 31	CEN MS 30	CEN MS 29	CEN MS 28	CEN MS 27-20	CEN MS 19	CEN MS 18	CEN MS 17	CEN MS 16

TABLE 13

Change Enable Least Significant Register (Base + 9A hex)

15	14	13	12	11-4	3	2	1	0
CEN LS 15	CEN LS 14	CEN LS 13	CEN LS 12	CEN LS 11-4	CEN LS 3	CEN LS 2	CEN LS 1	CEN LS 0

FIFO (Base + 9C, 9E hex)

The FIFO contains the states of the 32 input data lines at the time one of the data bits changed, followed by a 32 bit time value. The oldest data / time pair that the board contains will be read out when the VME bus reads the FIFO. The status of the FIFO should be checked before reading the FIFO, to make sure that valid data is available. The word format for the FIFO is shown below in Tables 14 & 15.

TABLE 14

FIFO Most Significant Register (Base + 9C hex)

15	14	13	12	11-4	3	2	1	0
FIFO MS 31	FIFO MS 30	FIFO MS 29	FIFO MS 28	FIFO MS 27-20	FIFO MS 19	FIFO MS 18	FIFO MS 17	FIFO MS 16

TABLE 15

FIFO Least Significant Register (Base + 9E hex)

15	14	13	12	11-4	3	2	1	0
FIFO LS 15	FIFO LS 14	FIFO LS 13	FIFO LS 12	FIFO LS 11-4	FIFO LS 3	FIFO LS 2	FIFO LS 1	FIFO LS 0