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PAS 9782/GEN
ENGINEERING SPECIFICATION

EIGHT CHANNEL VME
SINE/PULSE GENERATOR CARD
Revision B (06/29/09)

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Eight Channel VME
Sine/Pulse Generator Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9782/GEN is a VME based, eight channel function generator card. Each channel contains a Direct Digital Synthesis (DDS) chip that can be programmed to generate sine wave output signals. This DDS device is a Numerically Controlled Oscillator (NCO), employing a phase accumulator, a sine look-up table and a 10 bit D/A converter. The input clock frequency to the DDS chips is 2 MHz. This input frequency combined with the chips thirty-two bit phase accumulator provides a frequency resolution of 0.000465 Hz. The maximum useable output frequency is approximately 40 KHz.

A programmable gain amplifier is provided on each channel, following the NCO. This allows the card to be programmed for full-scale output ranges from +/-1 volt to +/-10 volts. In addition to the sine wave output a TTL output and open drain FET output are provided on each channel.

This card can be used in VME systems with A16, A24, or A32 addressing, and data bus widths of 16 and 32 bits are supported. DIP switches are used to configure the width of the address bus. VME instruction types determine the width of the data bus. The output signals are connected to a pair of DB37 female connectors mounted through the front panel. A board identifier PROM, control register and DDS frequency control registers are provided as well.

Card Features: PAS 9782/GEN

- 8 channel Direct Digital Synthesis (DDS) Waveform Generator
- Each channel provides sine wave, TTL square wave and open drain FET outputs
- Programmable Gain Amplifier per channel provides sine wave output of +/-10V, +/-5V, +/-2V or +/-1 volt peak to peak
- Output frequency is controlled by a 32 bit frequency register; each channel provides an independent frequency register
- Output frequency is set by the following equation: F(out) = F register value x 2 MHz divided by 2^32
- Each channel is controlled by two independent 12 bit phase offset registers
- All channels are clocked by a common 2 MHz crystal controlled oscillator
- Sine wave output amplifiers provide a low pass filter with a 3dB corner frequency of 30 KHz
- VME 6U form factor, 233mm x 160mm card size
- VME access: A32, A24, A16; D16 slave – No VME interrupts
- Board provides ID code (VMEIDPAS9782GENA), control and status register and two status LEDs
- Operating temperature range 0 to 60 degrees Celsius

II. SPECIFICATIONS

Electrical Specifications

General Information

Number of Sine/Pulse Out Channels	8
DDS Component	Analog Devices PN: AD9831 (see data sheet for additional info)

Output Characteristics

Sine Outputs

Voltage Ranges	+/-1V, +/-2 Volts, +/-5 Volts, +/-10 Volts
Output Current	+/-15 mA (typ)
Short-Circuit Current	+/-40 mA (typ)
Low Pass Corner Frequency	31 KHz

TTL Outputs

Low Level Output Current	10 mA
High Level Output Current	-10 mA
Low Level Output Voltage @ IOL = 4 mAmps	0.40 V (typ.), 0.6 V (max.)
High Level Output Voltage @ IOH = -1 mA	3.6 V (min.), 3.9 V (typ.)
High Level Output Voltage @ IOH = -10 mA	3.4 V (min.), 3.8 V (typ.)

FET Outputs

Pull-up Resistor	10 mA
Pull-up Voltage	+30 Volts (max)
Sink Current	100 mA (typ)

Card Power Requirements	5 Volts @ 1 Amp (typ)
VMEbus Compliance	Fully compatible with VMEbus standard
Address Range	A32, A24, and A16 switch selectable
Address Block Size	256 consecutive byte locations
Data Width	D16
Interrupts	none

Environmental Specifications

Operating Temperature Range	0 to 60 degrees Celsius
Storage Temperature Range	-40 to 85 degrees C.
Relative Humidity Range	0% to 100%, non-condensing

Physical Specifications

Dimensions	Form factor: 6U (160 mm x 233 mm)
Weight	12 oz. (typ)
Connectors	2 ea. 96 pos. DIN (VME bus connectors) 2 ea. DB37 female (Sine/Pulse Outputs) 1 ea. 6 pin shrouded header (reference and power supply voltages) Mating connector = Molex p/n 50-57-9406

Jumpers and Switches

The 9782/GEN card contains two eight position DIP switches, one ten-position DIP switch and eleven jumper plugs. The three DIP switches are used to set the board's VME base address, and are defined in Table 2 on page 10. When a switch is closed, the corresponding address bit must be low to select the card's address, and when a switch is open, the corresponding address bit must be high. The card is shipped configured for address F0000000.

Switches S2-9 and S2-10 are used to select the boards operating environment, A16, A24 or A32, and the setting of these switches is defined in table 1.

TABLE 1

Address Modifiers

JP10	S2-10	S2-9	Address Modifiers	Address Space
Out	Closed	Closed	09, 0D	Extended I/O
Out	Closed	Open	29,2D	Short I/O
Out	Open	Closed	39, 3D	Standard I/O
Out	Open	Open	29, 2D	Short I/O
In	Closed	Closed	0D	Extended I/O
In	Closed	Open	2D	Short I/O
In	Open	Closed	3D	Standard I/O
In	Open	Open	2D	Short I/O

Jumper plugs JP1 through JP8 are used to select the source of the pull up voltage for the open drain FET output on channels 1 through 8 respectively. When the jumpers are in position 1 to 2, the pull up resistors are connected to the external voltage pins in the DB37 connectors. When the jumpers are in position 2 to 3, the pull up resistors are connected to the +15 volt power supply.

Jumper plugs 9 through 11 control SYSFAIL, AM2 and the source of the master clock as described in the table 3.

TABLE 2

Switch Definitions

Switch	Function	Switch	Function
SW1-1	A8	SW2-5	A20
SW1-2	A9	SW2-6	A21
SW1-3	A10	SW2-7	A22
SW1-4	A11	SW2-8	A23
SW1-5	A12	SW3-1	A24
SW1-6	A13	SW3-2	A25
SW1-7	A14	SW3-3	A26
SW1-8	A15	SW3-4	A27
SW2-1	A16	SW3-5	A28
SW2-2	A17	SW3-6	A29
SW2-3	A18	SW3-7	A30
SW2-4	A19	SW3-8	A31

TABLE 3

Jumper Definitions

Jumper	Function
JP1	Channel 1 Pull-up Voltage Select
JP2	Channel 2 Pull-up Voltage Select
JP3	Channel 3 Pull-up Voltage Select
JP4	Channel 4 Pull-up Voltage Select
JP5	Channel 5 Pull-up Voltage Select
JP6	Channel 6 Pull-up Voltage Select
JP7	Channel 7 Pull-up Voltage Select
JP8	Channel 8 Pull-up Voltage Select
JP9	SYSFAIL controlled by control register
JP10	Enables AM2 (Refer to table 1)
JP11, 1-2	Use SYSCLK as master 16 MHz clock
JP11, 2-3	Use on-board 16 MHz oscillator

LED Indicators

Two LEDs are provided at the front panel to indicate the board's status. The upper red LED is the FAIL LED, and powers up on. This LED is controlled with bit 0 of the control register, and can be turned off by writing a one to that bit. The SYSFAIL line will also be driven when the FAIL LED is on, if JP9 is installed.

The lower green LED is the PASS LED, and its function is controlled by bit 1 of the control register. This LED can be turned on by writing a one to bit 1, and it will power up turned off. This LED can be used to indicate the board has passed some initial power up tests.

Connector Definitions

Two 96 position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. A pair of DB37 female connectors is installed through the board's front panel to provide access to eight sine/pulse output channels. A six position shrouded header is provided between the DB37 connectors to provide access to the reference voltages and power supplies. The pin out of these connectors is defined below and on the following page.

TABLE 4

6 Position Shrouded Header, P6

Pin #	Signal Name
1	Reference Voltage High
2	Analog Ground
3	-0.500 Volts
4	+15 VA
5	Analog Ground
6	-15 VA

TABLE 5

DB37 Connectors

			(P4)	(P3)
		19	AGND	AGND
AGND	37			
		18	EXTV4	EXTV8
GND	36			
		17	HV04	HV08
GND	35			
		16	TTL4	TTL8
GND	34			
		15	SINE4	SINE8
AGND	33			
		14	EXTV3	EXTV7
GND	32			
		13	HV03	HV07
GND	31			
		12	TTL3	TTL7
GND	30			
		11	SINE3	SINE7
AGND	29			
		10	EXTV2	EXTV6
GND	28			
		9	HV02	HV06
GND	27			
		8	TTL2	TTL6
GND	26			
		7	SINE2	SINE6
AGND	25			
		6	EXTV1	EXTV5
GND	24			
		5	HV01	HV05
GND	23			
		4	TTL1	TTL5
GND	22			
		3	SINE1	SINE5
AGND	21			
		2	AGND	AGND
AGND	20			
		1	AGND	AGND

III. PROGRAMMING INFORMATION

The PAS 9782/GEN card responds to word transfers to the control register set. The card's memory map is shown below, and occupies 256 bytes of VME memory.

TABLE 6

PAS 9782/GEN MEMORY MAP

BASE A+000	RESERVED	V (56)	001
002	RESERVED	M (4D)	003
004	RESERVED	E (45)	005
006	RESERVED	I (49)	007
008	RESERVED	D (44)	009
00A	RESERVED	P (50)	00B
00C	RESERVED	A (41)	00D
00E	RESERVED	S (53)	00F
000	RESERVED	9 (39)	011
012	RESERVED	7 (37)	013
014	RESERVED	8 (38)	015
016	RESERVED	2 (32)	017
018	RESERVED	G (47)	019
01A	RESERVED	E (45)	01B
01C	RESERVED	N (4E)	01D
01E	RESERVED	A (41)	01F
020	RESERVED	RESERVED	021
03E	RESERVED	RESERVED	03F
040	RESERVED	CONTROL & STATUS	041
050	Channel Control Registers	CCR1	051
052	Channel Control Registers	CCR2	053
054	Channel Control Registers	CCR3	055
056	Channel Control Registers	CCR4	057
058	Channel Control Registers	CCR5	059
05A	Channel Control Registers	CCR6	05B
05C	Channel Control Registers	CCR7	05D
05E	Channel Control Registers	CCR8	05F
060	RESERVED	RESERVED	061
07E	RESERVED	RESERVED	07F
080	CHANNEL 1	FREQ 0 REG 16 LSBs	081
082	CHANNEL 1	FREQ 0 REG 16 MSBs	083
084	CHANNEL 1	FREQ 1 REG 16 LSBs	085
086	CHANNEL 1	FREQ 1 REG 16 MSBs	087
088	CHANNEL 1	PHASE 0 REG	089
08A	CHANNEL 1	PHASE 1 REG	08B
08C	CHANNEL 1	PHASE 2 REG	08D
08E	CHANNEL 1	PHASE 3 REG	08F
090	CHANNEL 2	REGISTER SET	09F
0A0	CHANNEL 3	REGISTER SET	0AF
0B0	CHANNEL 4	REGISTER SET	0BF
0C0	CHANNEL 5	REGISTER SET	0CF
0D0	CHANNEL 6	REGISTER SET	0DF
0E0	CHANNEL 7	REGISTER SET	0EF
0F0	CHANNEL 8	REGISTER SET	0FF

Board Identifier PROM (Base Address + 001H to 01FH) Read Only

The Board Identifier PROM is located starting at the board's base address plus 1, and continues to the base address plus 1F.

Byte and word reads to the Identifier PROM are supported. Only the least significant byte of a word read will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

Control & Status Register (Base Address + 041) Read / Write

The Control & Status Register, (CSR), provides four bits that are used to set the states of the front panel LED's, enable the 2 MHz clock signal and reset the board. The format of this register is shown below.

TABLE 7

Control & Status Register

7	6	5	4	3	2	1	0
Loop Back	Loop Back	Loop Back	Soft Reset	Loop Back	2 MHz Enable	Pass LED	Fail LED

Bit 0 of the CSR steers the Fail LED at the front panel. The SYSFAIL line on the backplane will also be asserted if JP9 is installed, and bit 0 is reset. When the card is reset the Fail LED will come on. Writing a one to bit 0 will turn off the LED and the SYSFAIL line. Reading bit 0 returns the state that was last written.

Bit 1 of the CSR controls the Pass LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 will turn on the LED. Reading bit 1 returns the state that was last written.

Bit 2 of the CSR enables the 2 MHz clock signal to the DDS generator chips. This bit powers up reset, so it must be written to a one in order for the card to generate any output signals. Reading this bit returns the value that was last written.

Bit 4 of the CSR controls the software reset function. Writing a one to bit 4 will reset the board with a pulse. Reading bit 4 will return the value that was last written.

Bit 3, 5, 6 and 7 of the CSR will return the value that was last written. These bits have no other functions.

Channel Control Registers (Base Address + 051 thru 05F) Read / Write

The Channel Control Registers (CCR) are used to set the gain of the output amplifier, and to select the source of the frequency and phase offset registers. The format of these registers is shown below.

TABLE 8

Channel Control Register

7	6	5	4	3	2	1	0
Read Zero	Read Zero	Read Zero	Read Zero	Phase Select	Freq Select	Gain 1	Gain 0

Bit 0 and 1 of the CCR are used to select the gain of the output amplifier for the sine wave output. The gain and output voltage are shown in the table below.

Gain 1	Gain 0	Gain	Output Voltage
0	0	1	+/- 1 Volt
0	1	2	+/- 2 Volts
1	0	5	+/- 5 Volts
1	1	10	+/- 10 Volts

Reading these bits will return the value last written.

Bit 2 of the CCR is used to select which registers control the output frequency. Each DDS chip has two, 32 bit frequency control registers. When bit 2 is a zero it selects frequency register zero, and when it is a one, selects frequency register one. Reading this bit will return the value last written.

Bit 3 of the CCR is used to select which register will be used to control the phase offset. Each DDS chip has four, 12 bit phase offset registers. This card only provides access to two of the phase offset registers. When bit 3 is a zero it selects phase register zero, and when it is a one, selects phase register one. Reading this bit will return the value last written.

Bit 4 through 7 of the CCR have no function and will always return zeros when they are read.

Frequency Control Registers / Write Only (Base Address + 080–087, 090–097, 0A0–0A7, 0B0–0B7, 0C0–0C7, 0D0–0D7, 0E0–0E7, 0F0–0F7)

Each DDS chip contains two, 32 bit frequency control registers. The output frequency is determined by the value in the frequency register divided by 2^32 and multiplied by 2 MHz. The register that is used to set the frequency is determined by bit 2 in the CCR. In order to generate output frequencies, bit 2 in the CSR must be set to a one in order to enable the 2 MHz clock source to the DDS chips.

Phase Control Registers / Write Only (Base Address + 088–08F, 098–09F, 0A8–0AF, 0B8–0BF, 0C8–0CF, 0D8–0DF, 0E8–0EF, 0F8–0FF)

Each DDS chip contains four, 12 bit phase control registers. This card only allows selecting phase offset registers zero and one. These registers can be used to modulate the phase of the output waveform.