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PAS 9797/DIO
ENGINEERING SPECIFICATION

160 CHANNEL VME DIGITAL
INPUT / OUTPUT CARD
PCB REV C (05/04/07)

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160 Channel
VME Digital Input / Output Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9797/DIO is a VME based, 160 Channel, TTL level, Digital Input / Output card. One hundred twenty eight channels are arranged as sixteen, byte wide bi-directional data ports. These are the primary data ports and support 32 bit transfers. The remaining thirty two channels are arranged as four byte wide bi-directional data ports. Each port consists of an eight bit output data register with output enable, and an eight bit input buffer. The input buffers always monitor the state of the I/O lines, and the output data registers can either drive the I/O lines, or disconnect from the I/O by assuming a high impedance state. Individual data ports can be programmed for input or output by clearing or setting the appropriate bits in the output enable registers. When the data port is configured as an output, the state of the output lines can be read back with the input register.

The channels are divided into four blocks of 40 channels. Each block of I/O lines is terminated on a 50 position shrouded header at the card's front panel. The channels in each block consist of four byte wide bi-directional primary data ports, and eight additional I/O lines. The additional lines are from the B4, B5, D4 and D5 registers. Signals from these registers can be used as strobes and status lines for the primary data ports, or as general purpose I/O lines.

VME systems with A16, A24, or A32 addressing, and data bus widths of 8, 16 and 32 bits are supported. Thirty-two bit transfers are only supported by the primary data ports. The other registers on the card use byte or word transfers. DIP switches are used to configure the width of the address bus, and the instruction determines the width of the data transfer. A board identifier PROM and Control & Status register are also provided.

Card Features: PAS 9797/DIO

- 160 TTL level I/O signals arranged as, 128 primary general purpose I/O, 32 strobe or general purpose I/O
- General purpose I/O arranged as16 byte wide bi-directional data ports
- Additional I/O arranged as 4 byte wide bi-directional data ports
- Input / Output lines are terminated on 2, dual 50 position shrouded headers at the front panel
- All output signal lines have high current, 64 mA, sink current capability
- Board identifier PROM; ID code is VMEID PAS9797DIO *. (* Is revision level)
- SYSFAIL LED and Pass LED at the front panel
- VME SYSFAIL assert on power up, jumper selectable
- VME access: D32, D16, D8; A32, A24, A16 Slave
- VME interrupts; none
- VME 6U form factor; 233 mm x 160 mm card size.

II. SPECIFICATIONS

Electrical Specifications

Number of I/O Channels	160

Output Characteristics

Low Level Output Current	64 mA
High Level Output Current	-15 mA
Low Level Output Voltage @ IOL = 64 mAmps	0.35 V (typ.), 0.5 V (max.)
High Level Output Voltage @ IOH = -3 mA	2.4 V (min.), 3.2 V (typ.)
High Level Output Voltage @ IOH = -15 mA	2.0 V (min.)
Output Polarity	High True

Input Characteristics

High Level Input Voltage	2.0 V (min.)
Low Level Input Voltage	0.8 V (max.)
High Level Input Current @ V In = 2.7 V	20 uA (max.)
Low Level Input Current @ V In = 0.4 V	-0.7 mA (max.)

Note: All inputs are pulled up to + 5 Volts with 10 K Ohms. The low level input current includes -0.5 mA of current that flows through the resistor.

Card Power Requirements	5 Volts @ 1 Amp (typ)
VMEbus Compliance	Fully compatible with VMEbus standard
Address Range	A32, A24, A16 switch selectable
Address Block Size	2 K consecutive byte locations
Data Width	D32, D16, D8
Interrupts	none

Environmental Specifications

Operating Temperature Range	-20 to +71 degrees Celsius with forced Air-cooling.
Storage Temperature Range	-40 to 85 degrees C.
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: 6U (160 mm x 233 mm)
Weight	13 oz. (typ), 16 oz. (max)
Connectors	2 ea. 96 pos. DIN (VME bus connectors) 2 ea. Dual 50 pos. shrouded headers, (Input / Output data connectors)

The 9797/DIO card contains three jumper plugs, four sets of DIPswitches and four LED indicators.

Address Selection Switches (SW 1 through SW 4)

The DIPswitches are used to set the board's VME base address, and are defined in Table 2 on page 10. When a switch is closed, the corresponding address bit must be low to select the card's address. When a switch is open the corresponding address bit must be high. The card is shipped configured for address F0000000.

Two nine position DIP switches, (SW1 and SW2) are used to select the least significant bits of the base addresses for each half of the card. Switches 3 and 4 are used to define the most significant 16 bits of address decode.

Positions 1,2 and 3 of SW1 an SW2 are not used on this card. (They are used to select the interrupt level on a different version of the board.) The remaining 6 positions, labeled 4 through 9 on the switch, are used to select the cards base address. SW1 is used to select the base address of the A and B ports on the card. The connectors for these ports are located directly above the PCB. SW2 is used to select the base address of the C and D ports. The connectors for these ports are located directly above the connectors for the A and B ports.

Switch 3 is used to define address bits 24 through 31, and is only used for extended addressing. Switch 4 is used to define address bits 16 through 23, and is used for standard and extended addressing. The relationship between the base address bits and the switch setting is shown below.

Positions 9 and 10 of SW4 are used to select the board’s operating environment, either A16, A24 or A32. J3 is used in combination with SW4-9 and SW4-10 to determine which address modifiers to board responds to, as defined in TABLE 1. More information on J3 is provided in the section on jumpers.

TABLE 1

Address Modifiers

SW4-10	SW4-9	J3	Address Modifiers	Address Space
CLOSED	CLOSED	IN	0D	Extended I/O
CLOSED	CLOSED	OUT	09, 0D	Extended I/O
CLOSED	OPEN	IN	2D	Short I/O
CLOSED	OPEN	OUT	29, 2D	Short I/O
OPEN	CLOSED	IN	3D	Standard I/O
OPEN	CLOSED	OUT	39, 3D	Standard I/O
OPEN	OPEN	IN	2D	Short I/O
OPEN	OPEN	OUT	29, 2D	Short I/O

TABLE 2

Address Decode Switch Definitions

Switch #	Address Bit
SW1, 2-4	A10
SW1, 2-5	A11
SW1, 2-6	A12
SW1, 2-7	A13
SW1, 2-8	A14
SW1, 2-9	A15
SW4-1	A16
SW4-2	A17
SW4-3	A18
SW4-4	A19
SW4-5	A20
SW4-6	A21
SW4-7	A22
SW4-8	A23
SW3-1	A24
SW3-2	A25
SW3-3	A26
SW3-4	A27
SW3-5	A28
SW3-6	A29
SW3-7	A30
SW3-8	A31

Jumpers

Jumper J3 is used to configure to board to respond only to Supervisor access or to respond to both Non - Privileged and Supervisor accesses. When J3 is installed, the board only responds to Supervisor accesses. When J3 is removed, the board responds to both Non – Privileged and Supervisor accesses.
The board is shipped with J3 installed.

Jumper J19 is used to select the source of the board's master clock. In position 1-2, the clock is supplied from the VME backplane clock. In position 2-3, the clock is supplied from the onboard oscillator. The board is shipped with a jumper wire soldered from position 1 to 2.

Jumper J28 allows the SYSFAIL line to be driven with bit 0 of the control register when it is installed. The board is shipped with J28 installed.

LED Indicators

Four LED's are provided at the front panel to indicate the board's status. Two LED's are provided for each half of the card and are controlled by the CSR for that half of the card.

The upper two red LED's are the Fail LED's, and power up on. These LED's are controlled with bit 0 of the control registers, and can be turned off by writing a one to those bits. The SYSFAIL line will also be driven when either Fail LED is on, if J28 is installed.

The lower two green LED's are the Pass LED's, and power up off. These LED's are controlled by bit 1 of the control registers, and can be turned on by writing a one to those bits. These LED's can be used to indicate the board has passed some initial power up tests.

Connector Definitions

Two 96 position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. P1 is the upper connector and connects to the first 16 data lines, 24 address lines and the control signals. P2 is the lower connector, and connects to an additional 16 data lines and 8 address lines to complete the A32, D32 VMEbus interface.

Two dual 50 position shrouded headers are installed through the board's front panel to provide access to the I/O channels. The top connector is P3, and it terminates ports C and D. The lower connector is P4, and it terminates ports A and B. The pin out of these connectors is defined on the following pages.

TABLE 3

P3 Connector Definitions

P3A (On the PCB)

GND	50	49	GND
GND	48	47	GND
PB4-7	46	45	PB5-7
PB3-7	44	43	PB3-6
PB3-5	42	41	PB3-4
PB3-3	40	39	PB3-2
PB3-1	38	37	PB3-0
GND	36	35	GND
PB4-6	34	33	PB5-6
PB2-7	32	31	PB2-6
PB2-5	30	29	PB2-4
PB2-3	28	27	PB2-2
PB2-1	26	25	PB2-0
GND	24	23	GND
PB4-5	22	21	PB5-5
PB1-7	20	19	PB1-6
PB1-5	18	17	PB1-4
PB1-3	16	15	PB1-2
PB1-1	14	13	PB1-0
GND	12	11	GND
PB4-4	10	9	PB5-4
PB0-7	8	7	PB0-6
PB0-5	6	5	PB0-4
PB0-3	4	3	PB0-2
PB0-1	2	1	PB0-0

TABLE 4

P3 Connector Definitions

P3B (Above P3A)

GND	50	49	GND
GND	48	47	GND
PD4-7	46	45	PD5-7
PD3-7	44	43	PD3-6
PD3-5	42	41	PD3-4
PD3-3	40	39	PD3-2
PD3-1	38	37	PD3-0
GND	36	35	GND
PD4-6	34	33	PD5-6
PD2-7	32	31	PD2-6
PD2-5	30	29	PD2-4
PD2-3	28	27	PD2-2
PD2-1	26	25	PD2-0
GND	24	23	GND
PD4-5	22	21	PD5-5
PD1-7	20	19	PD1-6
PD1-5	18	17	PD1-4
PD1-3	16	15	PD1-2
PD1-1	14	13	PD1-0
GND	12	11	GND
PD4-4	10	9	PD5-4
PD0-7	8	7	PD0-6
PD0-5	6	5	PD0-4
PD0-3	4	3	PD0-2
PD0-1	2	1	PD0-0

TABLE 5

P4 Connector Pin Definitions

P4A (On the PCB)

GND	50	49	GND
GND	48	47	GND
PB4-3	46	45	PB5-3
PA3-7	44	43	PA3-6
PA3-5	42	41	PA3-4
PA3-3	40	39	PA3-2
PA3-1	38	37	PA3-0
GND	36	35	GND
PB4-2	34	33	PB5-2
PA2-7	32	31	PA2-6
PA2-5	30	29	PA2-4
PA2-3	28	27	PA2-2
PA2-1	26	25	PA2-0
GND	24	23	GND
PB4-1	22	21	PB5-1
PA1-7	20	19	PA1-6
PA1-5	18	17	PA1-4
PA1-3	16	15	PA1-2
PA1-1	14	13	PA1-0
GND	12	11	GND
PB4-0	10	9	PB5-0
PA0-7	8	7	PA0-6
PA0-5	6	5	PA0-4
PA0-3	4	3	PA0-2
PA0-1	2	1	PA0-0

TABLE 6

P4 Connector Pin Definitions

P4B (Above P4A)

GND	50	49	GND
GND	48	47	GND
PD4-3	46	45	PD5-3
PC3-7	44	43	PC3-6
PC3-5	42	41	PC3-4
PC3-3	40	39	PC3-2
PC3-1	38	37	PC3-0
GND	36	35	GND
PD4-2	34	33	PD5-2
PC2-7	32	31	PC2-6
PC2-5	30	29	PC2-4
PC2-3	28	27	PC2-2
PC2-1	26	25	PC2-0
GND	24	23	GND
PD4-1	22	21	PD5-1
PC1-7	20	19	PC1-6
PC1-5	18	17	PC1-4
PC1-3	16	15	PC1-2
PC1-1	14	13	PC1-0
GND	12	11	GND
PD4-0	10	9	PD5-0
PC0-7	8	7	PC0-6
PC0-5	6	5	PC0-4
PC0-3	4	3	PC0-2
PC0-1	2	1	PC0-0

III. PROGRAMMING INFORMATION

The 9797/DIO card responds to byte, word and longword transfers to the data port registers. Word and byte transfers to the control registers and the board identifier PROM are also supported. An example of the card's memory map is shown below, and indicates that this card appears as two copies of a card that occupies 1 Kbyte of VME memory, for a total of 2 Kbytes. This memory does not have to be in contiguous address space and two sets of address switches are provided for addressing each half of the card. The same ID PROM is selected for both the high and low 1 Kbyte block. All of the other registers decode unique addresses.

TABLE 7

PAS 9797/DIO MEMORY MAP

BASE A+ 000	RESERVED	V (56)	001
002	RESERVED	M (4D)	003
004	RESERVED	E (45)	005
006	RESERVED	I (49)	007
008	RESERVED	D (44)	009
00A	RESERVED	P (50)	00B
00C	RESERVED	A (41)	00D
00E	RESERVED	S (53)	00F
000	RESERVED	9 (39)	011
012	RESERVED	7 (37)	013
014	RESERVED	9 (39)	015
016	RESERVED	7 (37)	017
018	RESERVED	D (44)	019
01A	RESERVED	I (49)	01B
01C	RESERVED	O (4F)	01D
01E	RESERVED	A (41)	01F
020	RESERVED	RESERVED	021
07E	RESERVED	RESERVED	07F
080	RESERVED	CONTROL & STATUS	081
082	RESERVED	RESERVED	083
084	DATA PORT B4	RESERVED	085
086	DATA PORT B5	OUTPUT ENABLE	087
088	DATA PORT A0	DATA PORT A1	089
08A	DATA PORT A2	DATA PORT A3	08B
08C	DATA PORT B0	DATA PORT B1	08D
08E	DATA PORT B2	DATA PORT B3	08F
090	RESERVED	RESERVED	091
3FE	RESERVED	RESERVED	3FF

TABLE 7 CONT.

PAS 9797/DIO MEMORY MAP

BASE C+ 000	RESERVED	ID PROM	001
01E	RESERVED	ID PROM	01F
020	RESERVED	RESERVED	021
07E	RESERVED	RESERVED	07F
080	RESERVED	CONTROL & STATUS	081
082	RESERVED	RESERVED	083
084	DATA PORT D4	RESERVED	085
086	DATA PORT D5	OUTPUT ENABLE	087
088	DATA PORT C0	DATA PORT C1	089
08A	DATA PORT C2	DATA PORT C3	08B
08C	DATA PORT D0	DATA PORT D1	08D
08E	DATA PORT D2	DATA PORT D3	08F
090	RESERVED	RESERVED	091
3FE	RESERVED	RESERVED	3FF

Board Identifier PROM (Base Address A + 001H to 01FH) Read Only Second Copy (Base Address C + 001H to 41FH)

The Board Identifier PROM is located starting at the board's base address plus 1, and continues to the base address plus 1F. Another range of addresses starting from the second base address plus 1 is decoded to read the ID PROM. Both address ranges decode to select the same PROM.

Byte and word reads to the Identifier PROM are supported. Only the least significant byte of a word read will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

Control & Status Register (Base Address A + 081H) Read / Write
Second Copy (Base Address C + 081H)

The Control & Status Register, (CSR), provides two bits that are used to set the states of the front panel LED's and SYSFAIL line, a software reset bit, two port enable bits, and three loopback bits. Two copies of the CSR are provided, and they are addressed at offset 081 from the base addresses. The format of these registers is shown below.

TABLE 8

Control & Status Register

7	6	5	4	3	2	1	0
Loop Back	Enbl B5,D5	Enbl B4,D4	Soft Rst	Loop Back	Loop Back	Pass LED	Fail LED

Bit 0 of the CSR steers the Fail LED at the front panel. The SYSFAIL line on the backplane, will also be asserted if J28 is installed, and bit 0 is reset in either CSR. When the card is reset the Fail LED's will come on. The LED's and the SYSFAIL line can be turned off by writing a one to bit 0. Reading bit 0 returns the state that was last written.

Bit 1 of the CSR controls the Pass LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. The LED can be turned on by writing a one to bit 1. Reading bit 1 returns the state that was last written.

Bits 2 and 3 of the CSR are loopback bits and will return the value that was last written to them. These bits have no other function.

The software reset function is controlled by bit 4 of the CSR. When bit 4 is set to a logic 1, the card will be in the software reset state. In order to perform normal operations with the card, bit 4 must be reset to a logic 0. When soft ware reset is performed, the registers on the card will reset to the following states:

- The Primary Data Ports will all be configured as inputs
- The Primary Data Output Registers will be cleared to 00H
- The Additional I/O Ports will all be configured as inputs
- The Additional Output Registers will be cleared to 00H
- Reading bit 4 returns the value that was last written

Bit 5 enables the outputs on B4, D4 I/O Data Ports. Writing a logic 0 to this bit configures the port as an input by disabling the Output Registers. Writing a logic 1 configures the port for output. Reading this bit returns the value that was last written.

Bit 6 enables the outputs on B5, D5 I/O Data Ports. Writing a logic 0 to this bit configures the port as an input by disabling the Output Registers. Writing a logic 1 configures the port for output. Reading this bit returns the value that was last written.

Bit 7 of the CSR will return the value that was last written. This bit has no other function.

B4, D4 Input / Output Data Ports (Base Address A + 084H) Read / Write Second Address (Base Address C + 084H)

The B4 and D4 Input / Output Data Ports are byte wide bi-directional registers that are connected to the I/O lines. These registers can be configured for either input or output operation using the Control and Status Registers. Following a reset, all of the Data Ports are configured as Inputs. Reading the ports will return a one for each bit that has a corresponding I/O line in the high state, and a zero for inputs that are in the low state. When the Port is configured as an output, bits that are written with ones will cause the corresponding output lines to be driven to the high state, and zeros will produce the low state. The Data Port can be read back when it is configured as an output, and it will return the value that was written last. The format of the B4 and D4 Data Ports is shown below.

TABLE 9

B4 Input / Output Data Port

7	6	5	4	3	2	1	0
B4 Bit 7	B4 Bit 6	B4 Bit 5	B4 Bit 4	B4 Bit 3	B4 Bit 2	B4 Bit 1	B4 Bit 0

TABLE 10

D4 Input / Output Data Port

7	6	5	4	3	2	1	0
D4 Bit 7	D4 Bit 6	D4 Bit 5	D4 Bit 4	D4 Bit 3	D4 Bit 2	D4 Bit 1	D4 Bit 0

A logic 1 corresponds to a high state on the I/O Data line.
A logic 0 corresponds to a low state on the I/O Data line.

B5, D5 Input /Output Data Ports (Base Address A + 086H) Read / Write Second Address (Base Address C + 086H)

The B5 and D5 Input / Output Data Ports are byte wide bi-directional registers that are connected to the I/O lines. These registers can be configured for either input or output operation using the Control and Status Registers. Following a reset, all of the Data Ports are configured as Inputs. Reading the ports will return a one for each bit that has a corresponding I/O line in the high state, and a zero for inputs that are in the low state. When the Port is configured as an output, bits that are written with ones will cause the corresponding output lines to be driven to the high state, and zeros will produce the low state. The Data Port can be read back when it is configured as an output, and it will return the value that was written last. The format of the B5 and D5 Data Ports is shown below.

TABLE 11

B5 Input / Output Data Port

7	6	5	4	3	2	1	0
B5 Bit 7	B5 Bit 6	B5 Bit 5	B5 Bit 4	B5 Bit 3	B5 Bit 2	B5 Bit 1	B5 Bit 0

TABLE 12

D5 Input / Output Data Port

7	6	5	4	3	2	1	0
D5 Bit 7	D5 Bit 6	D5 Bit 5	D5 Bit 4	D5 Bit 3	D5 Bit 2	D5 Bit 1	D5 Bit 0

A logic 1 corresponds to a high state on the I/O Data line.
A logic 0 corresponds to a low state on the I/O Data line.

Output Enable Registers (Base Address A + 087H) Read / Write
Second Address (Base Address C + 087H)

The Output Enable Registers are used to configure the byte wide I/O ports for either input or output operation. Writing a one to an output enable bit configures that port as an output, and a zero configures it as an input. Reading these registers returns the last value that was written. During power up or in response to a software reset, these registers are cleared to all zeros, which specifies all of the ports as inputs. The format of the Output Enable Registers is shown below.

TABLE 13

Output Enable Register A

7	6	5	4	3	2	1	0
Outpt En B3	Outpt En B2	Outpt En B1	Outpt En B0	Outpt En A3	Outpt En A2	Outpt En A1	Outpt En A0

TABLE 14

Output Enable Register C

7	6	5	4	3	2	1	0
Outpt En D3	Outpt En D2	Outpt En D1	Outpt En D0	Outpt En C3	Outpt En C2	Outpt En C1	Outpt En C0

A logic 1 configures a port for output.
A logic 0 configures a port for input.

Input / Output Data Ports (Base Add A + 088H to 08FH) Read / Write Second Copies (Base Add C + 088H to 08FH)

The Input / Output Data Ports are byte wide bi-directional registers that are connected to the I/O data lines. These registers can be configured for either input or output operation using the Output Enable Registers. Following a reset, all of the Data Ports are configured as Inputs. Reading the ports will return a one for each bit that has a corresponding I/O line in the high state, and a zero for inputs that are in the low state. When the Data Port is configured as an output, bits that are written with ones will cause the corresponding output lines to be driven to the high state, and zeros will produce the low state. The Data Port can be read back when it is configured as an output, and it will return the value that was written last. The format of the I / O Data Ports is shown below.

TABLE 15

Input / Output Data Port

7	6	5	4	3	2	1	0
Data Bit 7	Data Bit 6	Data Bit 5	Data Bit 4	Data Bit 3	Data Bit 2	Data Bit 1	Data Bit 0

A logic 1 corresponds to a high state on the I/O line.
A logic 0 corresponds to a low state on the I/O line.