Document PAS0064

PAS 9816/AO
ENGINEERING SPECIFICATION

16 CHANNEL, 16 BIT
VME ANALOG OUTPUT CARD
Revision C1

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16 Channel 16 Bit
VME Analog Output Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9816/AO provides sixteen analog output channels with sixteen bit resolution on a standard 6U x 160mm VME card. Analog output voltage range is ± 10 Volts with ± 5 mAmp output current drive per channel. Settling time is 3 uSec typically and 4 uSec maximum.

This card is a software compatible, improved version of the PAS 9716/AO. Different Digital to Analog Converters are used on this card, and they provide the performance improvements. Both DAC's are made by Texas Instruments-Burr Brown. The PAS 9716/AO uses the DAC712 and the PAS 9816/AO used the newer DAC7742. Areas where performance is improved include settling time, glitch impulse, output noise and power consumption. A performance comparison is provided in Table 1. The PAS 9816/AO also allows the digital data that was last written to the D to A Converters to be read back over the VME bus. The PAS 9716/AO did not support this feature.

Analog output signals are available on a 37 position D connector mounted through the front panel. This connector also provides access to two general purpose digital output signals. VME systems with A16, A24 and A32 are supported, and DIP switches are used to set the cards address and address width. Data writes and reads of 16 and 32 bits are supported and selected by the instruction type. DAC's can be updated two at a time by using 32 bit writes.

Addition features include board identifier registers, control and status register, 32 bit test register and front panel status LED's.

TABLE 1
COMPARISON OF DAC 712 AND DAC 7742

	DAC 712	DAC7742
Settling Time	6 uSec (typ) 10 uSec (max)	3 uSec (typ) 4 uSec (max)
Glitch Impulse	15 nV – s (typ)	2 nV – s (typ)
Output Noise	120 nV / root Hz	100 nV / root Hz
Positive PS current	13 to 15 mA	4 to 6 mA
Negative PS current	22 to 25 mA	2.5 to 4 mA

Card Features: PAS 9816/AO

- 16 channels ,16 bit voltage outputs
- +/- 10 Volt @ 5 mAmp output
- Binary Two's Complement Data Format
- Digital read back of last value written to each DAC
- DAC's reset to bipolar zero during power up reset
- Output impedance of 0.1 ohm
- Output short circuit proof to analog ground
- Output slew rate of 10 Volts per uSec
- Settling time of 3 uSec to 0.003% FSR (5K ohm parallel with 200 pF load)
- VME 6U form factor; 233 mm x 160 mm card size
- VME access: D32, D16; A32, A24, A16 Slave
- No VME Interrupts
- Optional VME SYSFAIL assert on power up, jumper selectable
- Pass, Fail and board access LED's on the front panel
- Board Identifier PROM (Board ID is VMEID PAS9816/AO C1)
- Simultaneous DAC update feature is program selectable
- 2 Digital Output channels
- Output signals on DB 37 connector at the front panel
- Loop back test registers allow verification of the VME bus interface
- 32-bit VME interface allows two channels to be written with one transfer and provides twice the data transfer rate of 16 bit interfaces. 16-bit VME transfers are also supported
- DAC's are powered by the +/- 12 Volts from the VME bus or optional DC to DC converter
- Operating temperature range 0 to 60 degrees Celsius

II. SPECIFICATIONS

Electrical Specifications

Analog Outputs

Number of DAC Channels	16
DAC Type	DAC 7742Y, B, C
Resolution	16 bits
Output Voltage Range	± 10.000 Volts
LSB Weight	305 uVolt
Output Current	± 5 mAmps (min)
Settling Time	3 uSec (typ), 4 uSec (max)
20 V Output Step	
R = 5K ohm, C = 200 pF	
Zero Error	± 2 LSB (adjustable to zero)
Zero Error Drift	± 2 ppm / deg.C
Gain Error	± 0.01 % FS (adjustable to zero)
Gain Error Drift	± 15 ppm / deg. C (see below)
Output Impedence	0.1 Ohm (typ)
Maximum Load Capacitance	200 pF
Short to AGND Duration	Indefinite

Digital Outputs

Number of Digital Outputs	2
DO Driver Type	74F125
Low Level Output	0.40 V (typ), 0.55 V (max) @ I out = 64 mA
High Level Output Voltage	3.1 V (typ), 2.0 V (min) @ I out = -15 mA

Card Power Requirements	+ 5 Volts @ 1 Amp (typ)
(Backplane supplies ± 12 V)	+ 12 Volts @ 96 mA (no load)
	+ 12 Volts @ 176 mA (full load)
	- 12 Volts @ 64 mA (no load)
	-12 Volts @ 144 mA (full load)

PAS 9816/AO-000	**DAC7742Y (DAC Type)**
DAC Integral Nonlinearity	± 5 LSB (max)
T min. to T max.	± 6 LSB (max)
DAC Differential Nonlinearity	± 4 LSB (max)
T min to T max.	± 4 LSB (max)
Monotonicity over Temp	14 Bits (min)
Gain Error Drift	± 15 ppm / deg C

PAS 9816/AO-010	**DAC7742YB (DAC Type)**
DAC Integral Nonlinearity	± 3 LSB (max)
T min. to T max.	± 4 LSB (max)
AC Differential Nonlinearity	± 2 LSB (max)
T min. to T max.	± 2 LSB (max)
Monotonicity over Temp	15 Bits (min)
Gain Error Drift	± 10 ppm / deg C

PAS 9816/AO-020	**DAC7742YC (DAC Type)**
DAC Integral Nonlinearity	± 2 LSB (max)
T min. to T max.	± 3 LSB (max)
DAC Differential Nonlinearity	± 1 LSB (max)
T min. to T max.	± 1 LSB (max)
Monotonicity over Temp	16 Bits (min)
Gain Error Drift	± 7 ppm / deg C

Environmental Specifications

Operating Temperature Range	0 to 60º C.
Storage Temperature Range	-20 to 85º C.
Relative Humidity Range	20% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	12 oz. (typ)
Connectors	2 ea. 96 position, (VME bus connectors) 1 ea. DB37 female, (Analog Output connector)

Switches and Jumper Plug Definitions

The PAS 9816/AO card contains three eight position DIP switches, one three position DIP switch, and one jumper plug. The three eight position DIP switches are used to set the card's VME address and are defined in Table 2 below. When a switch is closed or on, the corresponding address bit must be low to select the card's address, and when a switch is open or off, the corresponding address bit must be high.

Switches SW4-1 and 2 are used to select the card's operating environment; A16, A24, or A32. The setting of these switches is defined in Table 3 on page 10.

Switch SW4-3 is used to enable the software reset function when it is open or off. Software reset is disabled when SW4-3 is closed or on. For more information on the software reset function, see the control and status register in the programming information section.

The card is shipped configured for short space, address 1000 hex, with the software reset function enabled.

Jumper plug 2 controls the SYSFAIL line as described in Table 2.

TABLE 2

SWITCH AND JUMPER DEFINITIONS

Switch #	Function
SW1-1	A8
SW1-2	A9
SW1-3	A10
SW1-4	A11
SW1-5	A12
SW1-6	A13
SW1-7	A14
SW1-8	A15
SW2-1	A16
SW2-2	A17
SW2-3	A18
SW2-4	A19
SW2-5	A20
SW2-6	A21
SW2-7	A22
SW2-8	A23
SW3-1	A24
SW3-2	A25
SW3-3	A26
SW3-4	A27
SW3-5	A28
SW3-6	A29
SW3-7	A30
SW3-8	A31
J2 IN	SYSFAIL controlled by control register

TABLE 3

SWTICH DEFINITIONS

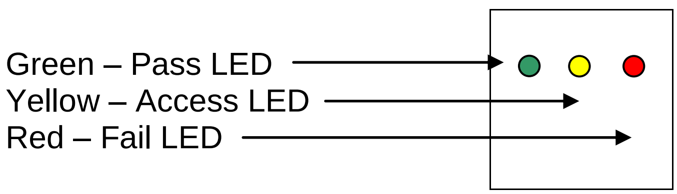
SW4-1	SW4-2	Address Modifiers	Address Space
Closed	Closed	09, 0D	Extended
Open	Closed	39, 3D	Standard
Closed	Open	29, 2D	Geographical *
Open	Open	29, 2D	Short

*Requires a special chassis

Front Panel LED Definitions

Three LED's are available at the front panel to indicate the board's status. The position of the LEDs is shown below.

Top of Front Panel



The Fail LED powers up on, and is controlled with bit 0 of the control register. Writing a one to bit 0 will turn off this LED. The state of this LED is reflected in bit 0 of the status register. When the Fail LED is on, and JP2 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the control register. This LED will be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the status register reflects the state of this LED. Once the board has passed some initial power up tests this LED can be turned on to indicate successful completion of the power up sequence. The yellow, access LED will turn on anytime the board is accessed.

Connector Definitions

Two 96 position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. A DB37 female connector is installed through the board's front panel to provide access to the sixteen analog output channels and the two digital outputs. The pin out of this connector is defined on the following page.

TABLE 4

DB37 CONNECTOR (P3)

AGND	37	19	AGND
AGND	36	18	CH1H
AGND	35	17	CH3H
AGND	34	16	CH5H
AGND	33	15	CH7H
AGND	32	14	CH9H
AGND	31	13	CH11H
AGND	30	12	CH13H
AGND	29	11	CH15H
AGND	28	10	CH0H
AGND	27	9	CH2H
AGND	26	8	CH4H
AGND	25	7	CH6H
AGND	24	6	CH8H
AGND	23	5	CH10H
AGND	22	4	CH12H
AGND	21	3	CH14H
AGND	20	2	DO1
		1	DO2

III. PROGRAMMING INFORMATION

The 9816/AO card responds to word and longword writes and reads to the sixteen Digital to Analog Converters (DAC's). The card also supports word writes and reads to the control and status register, and word reads of the board identifier registers. A thirty two-bit test register is provided, and it responds to word and longword transfers. The card's memory map is shown below.

<u>TABLE 5</u>

PAS 9816/AO MEMORY MAP

BASE +00	98	16	BASE + 01
02	Control/Status	Control/Status	03
04	Reserved	Reserved	05
06	Reserved	Reserved	07
08	Test Register	Test Register	09
0A	Test Register	Test Register	0B
0C	Reserved	Reserved	0D
0E	Reserved	Reserved	0F
10	Reserved	Reserved	11
12	Reserved	Reserved	13
14	Reserved	Reserved	15
16	Reserved	Reserved	17
18	Reserved	Reserved	19
1A	Reserved	Reserved	1B
1C	Reserved	Reserved	1D
1E	Reserved	Reserved	1F
20	00	V (56)	21
22	00	M (4D)	23
24	00	E (45)	25
26	00	I (49)	27
28	00	D (44)	29
2A	00	P (50)	2B
2C	00	A (41)	2D
2E	00	S (53)	2F
30	00	9 (39)	31
32	00	8 (38)	33
34	00	1 (31)	35
36	00	6 (36)	37
38	00	A (41)	39
3A	00	O (4F)	3B
3C	00	C (43)	3D
3E	00	1 (31)	3F
40	DAC CHANNEL 0	DAC CHANNEL 0	41
42	DAC CHANNEL 1	DAC CHANNEL 1	43
44	DAC CHANNEL 2	DAC CHANNEL 2	45
46	DAC CHANNEL 3	DAC CHANNEL 3	47
48	DAC CHANNEL 4	DAC CHANNEL 4	49
4A	DAC CHANNEL 5	DAC CHANNEL 5	4B
4C	DAC CHANNEL 6	DAC CHANNEL 6	4D
4E	DAC CHANNEL 7	DAC CHANNEL 7	4F
50	DAC CHANNEL 8	DAC CHANNEL 8	51
52	DAC CHANNEL 9	DAC CHANNEL 9	53
54	DAC CHANNEL 10	DAC CHANNEL 10	55
56	DAC CHANNEL 11	DAC CHANNEL 11	57
58	DAC CHANNEL 12	DAC CHANNEL 12	59
5A	DAC CHANNEL 13	DAC CHANNEL 13	5B
5C	DAC CHENNEL 14	DAC CHANNEL 14	5D
5E	DAC CHANNEL 15	DAC CHANNEL 15	5F
60	RESERVED	RESERVED	61
FE	RESERVED	RESERVED	FF

Fast ID Register (Base Address + 00H) Read Only

The fast ID register is located at the card's base address plus 00. Reads to this register will return the hex value 9816, which is the board's model number. Writing this register will handshake, but not transfer any data.

Control and Status Register (Base Address + 02H) Read/Write

TABLE 6

CONTROL AND STATUS REGISTER

15-7	6	5	4	3	2	1	0
Loop Back HT	Software Reset HT	Digital Output 2 HT	Digital Output 1 HT	Output Enable HT	Sim Update HT	Pass LED HT	Fail LED LT

LT = Low True
HT = High True

The Control and Status Register is located at the cards base address plus 02. Writes to the Control register are used to set the states of the LED's and the SYSFAIL line, to control the Digital Output lines, and to control the simultaneous update and software reset functions.

Bit 0 of the Control Register steers the Fail LED, and the SYSFAIL line on the backplane, if J2 is installed. When the card is reset the Fail LED will come on, and the SYSFAIL line will be driven true. The LED and the SYSFAIL line can be turned off by writing a one to bit 0. Reading bit 0 returns the state that was last written.

Bit 1 of the Control Register controls the Pass LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. The LED can be turned on by writing a one to bit 1. Reading bit 1 returns the state that was last written.

Bit 2 of the Control Register controls the simultaneous update feature. This function is disabled when the board is reset or when a zero is written to bit 2. When simultaneous update is disabled, the DAC's will be updated whenever they are written. Simultaneous update can be enabled by writing a one to bit 2, as part of the sequence described below on writing to the DAC's.

Bit 3 of the Control Register is used to enable the digital output drivers. The drivers are disabled when the board is reset or when a zero is written to bit 3. This puts the outputs in a high impedance state. The drivers are enabled by writing a one to bit 3.

Bits 4 and 5 of the Control Register control the state of Digital Outputs 1 and 2 respectively. The outputs will be low whenever a zero is written to these bits, and the outputs are enabled. When the card is reset, the outputs are disabled. The outputs will be driven high by writing ones to bits 4 or 5 with the outputs enabled.

Bit 6 in the Control Register controls the software reset function when enabled by SW4-3 being open. When bit 6 is written with a one with reset enabled, the reset pulse will be generated. Software reset causes all the DAC's to reset to zero volts, and clears the CSR and Test Register to all zeros. When the software reset function is disabled, bit 6 has no function, other than to loop back the value that was written last.

Bits 7 through 15 in the Control Register do not have any function, however they are returned in the status register.

The power up or reset condition of the Control and Status Register is 0000, and indicates the Digital Outputs are disabled, simultaneous update is disabled, the PASS LED is off, and the FAIL LED is on.

32 Bit Test Register (Base Address + 08) Read/Write

The 32-bit Test Register can be written to and read at the card's base address plus 08 (hex). This register supports word and long word transfers, and is useful for verifying the proper operation of the VME bus interface. Reading the register will return the value that was last written to it.

Board Identifier Registers (Base Address + 20H to 3EH) Read Only

The Board Identifier registers are located starting at the board's base address plus 20, and continues to the base address plus 3E.

Byte and word reads to the Identifier registers are supported. Only the least significant byte of a word read will contain valid data, and the most significant byte will contain 00. The ID registers contains 16 ASCII characters that specify the board's model number and revision level. Writes to the ID registers will handshake, but not transfer any data.

16 Bit Digital to Analog Converters (Base Address + 40H to 5EH) Read/Write

The sixteen D to A converters can be written to starting at the board's base address plus 40 (hex). Binary Two's Complement is the format of data written to the DAC's. For the bipolar Analog Output configuration of this card, a digital word of 7FFF gives positive full scale output, 8000 hex gives negative full scale output, and 0000 hex gives bipolar zero output.

Dual rank registers are used in the DAC's and data is always written into the DAC's input register. If simultaneous update is disabled, the DAC register will also be updated during this write.

If the DAC's are to be updated simultaneously, then the following sequence should be performed;

1) Bit 2 in the Control Register is set to a 1 to disable the DAC registers from tracking the input registers,
2) All but one of the DAC's are written to,
3) Bit 2 in the Control Register is set to zero,
4) The final DAC is written to. This will cause all of the DAC's to be updated on the final write.

The Digital to Analog Converters can be written to individually using word transfers, or in pairs using long word transfers. Reading the DAC's will return the status of their input registers. Word and long word reads are supported. By using long words, two DAC's can be read with a single transfer. During a power up reset, the output voltage of all of the DAC's will set to 0.000 Volts.

IV. CALIBRATION PROCEDURE

Install the 9816/AO card in a VME chassis, and allow the card to stabilize for approximately five minutes. A meter with five digits of resolution and accuracy is required to perform these adjustments.

Offset Adjustment

The offset adjustment should be performed before the gain adjustment to avoid interaction of adjustments. Write the hex value 0000 to the channel to be adjusted, and adjust the zero potentiometer for a value of 0.0000 Volts ± 100 uVolts. The zero adjustments are identified in the following table, and they are the pots closest to the front panel.

Gain Adjustment

Write a hex value of 7FFF to the channel to be adjusted, and adjust the gain potentiometer for a value of + 9.9996 Volts. The gain adjustments are identified in the following table, and they are located to the right, or inboard of the zero pots.

TABLE 7
OFFSET AND GAIN ADJUSTMENT POTENTIOMETERS

P3 Pin #	Channel #	Offset Adjustment	Gain Adjustment	Address	DAC
18	1	R15	R12	42	U16
17	3	R21	R18	46	U17
16	5	R27	R24	4A	U18
15	7	R33	R30	4E	U19
14	9	R39	R36	52	U20
13	11	R45	R42	56	U21
12	13	R51	R48	5A	U22
11	15	R57	R54	5E	U23
10	0	R63	R60	40	U24
9	2	R69	R66	44	U25
8	4	R75	R72	48	U26
7	6	R81	R78	4C	U27
6	8	R87	R84	50	U28
5	10	R93	R90	54	U29
4	12	R99	R96	58	U30
3	14	R105	R102	5C	U31