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PAS 9818/AO
ENGINEERING SPECIFICATION

VME 8 CHANNEL, 16 BIT PROGRAMMABLE CURRENT OUTPUT CARD
Revision A

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VME 8 Channel 16 Bit Programmable Current Output Card

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VME 8 Channel 16 Bit High Power
VME Analog Output Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9818/AO provides eight programmable current output channels with sixteen bit resolution on a 6U VME card. Each channel consists of a high speed Digital-to-Analog Converter (DAC), followed by a high power operational amplifier. The output amplifier is configured to provide an output current that is proportional to the output voltage from the DAC. The output current range is positive to negative forty mAmps. Each amplifier provides a flag indicator that sets when the amplifier is in an over-current fault condition. Power to the output amplifiers can either be provided externally, or by on-board DC-to-DC converters.

All of the output channels and the external power supply connections can be terminated on the P2 connector of the VME backplane. A DB37 connector mounted through the front panel is available as an option for terminating the output and power supply signals. Refer to the end of section II of this manual for ordering information.

The card can be used in VME systems with A16, A24, or A32 addressing, and data writes of 16 and 32 bits are supported. DIP switches are used to configure the width of the address bus, and the instruction type specifies the data bus width. A board identifier PROM, fast ID register, control and status register, flag register, and a 32-bit test register fill out the register set.

Card Features: PAS 9818/AO

- 8 independent DAC channels with 16 bit programmable current outputs
- +/- 40 mAmp current output
- Binary Two's Complement data format
- DAC's reset to zero during power up or software reset
- Output slew rate of 1 mAmp per uSec
- Settling time of 100 uSec to 0.1% FSR
- Each amplifier provides a flag signal that indicates the amplifier is in a fault condition. These signals can be accessed through software, by reading the flag register.
- Output signals and power supply terminate on P2 backplane connector, or on a DB37 connector at the front panel
- VME 6U form factor; 233 mm x 160 mm card size
- VME access: D32, D16, A32, A24, A16 Slave
- No VME Interrupts
- VME SYSFAIL asserts on power up, jumper selectable
- Board Identifier PROM (Board ID is VMEIDPAS9818AOA0)
- Pass and Fail LED's on the front panel
- Simultaneous DAC update feature is program selectable.
- Loop back test registers allow verification of the VME bus interface.
- 32-bit VME interface allows two channels to be written with one transfer and provides twice the data transfer rate of 16 bit interfaces. 16 bit VME transfers are also supported.
- DAC's are powered by the +/- 12 Volts from the VME bus, or by on-board DC-to-DC converters.
- Output amplifiers can be powered by external power supplies or by on-board DC-to-DC converters
- Operating temperature range 0 to 55 deg. C.

II. SPECIFICATIONS

Electrical Specifications

Number of Channels	8 Analog Outputs
Resolution	16 bits
Output Current	+/- 40 mAmps
LSB bit weight	1.22 uAmp
Settling Time	100 uSec to 0.1%(typ)

Standard Card

DAC Integral Nonlinearity	+/- 4 LSB (max.)
T min. to T max.	+/- 8 LSB (max.)
DAC Differential Nonlinearity	+/- 4 LSB (max.)
T min to T max.	+/- 8 LSB (max.)

Possible Future Option	-K Version DAC
DAC Integral Nonlinearity	+/- 2 LSB (max.)
T min. to T max.	+/- 2 LSB (max.)
AC Differential Nonlinearity	+/- 2 LSB (max.)
T min. to T max.	+/- 2 LSB (max.)

Possible Future Option	-L Version DAC
DAC Integral Nonlinearity	+/- 2 LSB (max.)
T min. to T max.	+/- 2 LSB (max.)
DAC Differential Nonlinearity	+/- 1 LSB (max.)
T min. to T max.	+/- 1 LSB (max.)

Zero Error	+/- 4 LSB (adjustable to zero)
Gain Error	+/- 0.05 % FS (adjustable to zero)

Card Power Requirements	5 Volts @ 1 Amp, (typ) - TBD
(Backplane power supplies)	+12 Volts @ 120 mAmps - TBD
	-12 Volts @ 200 mAmps - TBD

External Power Supply Voltage	+/- 10 Volts (min), +/- 40 Volts (max)
Amplifier Quiescent Current	100 mA (typ.), 150 mA (max)

Environmental Specifications

Operating Temperature Range	0 to 55 degrees C.
Storage Temperature Range	-20 to 85 degrees C.
Relative Humidity Range	0% to 80%, non-condensing

Physical Specifications

Dimensions	Form factor: Double (160 mm x 233 mm)
Weight	24 oz. (typ) - TBD
Connectors	2 ea. 96 position, (VME bus connectors) Analog Outputs on P2 a and c rows 1 ea. Optional DB37 female, (Analog Output connector)

Ordering Information

A three digit “dash number” specifies the configuration of the card. The three digits in the dash number are referred to as X, Y and Z. The dash number configurations are defined below.

X = **0** – Hot Swap Disabled / **1** – Hot Swap Enabled

Y = **0** – Output signals through P4 (DB37) @ front panel
1 – Output signals through P2 (96DIN) @ backplane

Z = **0** – External Power Source / **1** – +/-24 volt on-board power supply
2 – +/-30 volt on-board power supply

Example

Ordering model # *PAS 9818/AO-002* = Hot swap disabled, output signals going out through front panel and +/-30 volt on-board power supply.

Switches and Jumper Plug Definitions

The PAS 9818/AO card contains three eight position DIP switches, one three position DIP switch, and one jumper plug. The three eight position DIP switches are used to set the card's VME address and are defined in Table 1 on page 10. When a switch is closed or on, the corresponding address bit must be low to select the card's address, and when a switch is open of off, the corresponding address bit must be high.

Switches SW4-1 and 2 are used to select the cards operating environment, A16, A24 or A32. The setting of these switches is defined in Table 2 on page 10. SW4-3 has no function at this time and is reserved for future use.

Jumper plug 2 (JP2), controls the SYSFAIL line. When JP2 is installed SYSFAIL will be asserted at power up or after a system reset. The SYSFAIL line can be de-asserted by writing a one to bit zero of the CSR. When JP2 is removed, this card will not drive the SYSFAIL line.

TABLE 1

DIP SWITCH DEFINITIONS

Jumper #	Function
SW1-1	A8
SW1-2	A9
SW1-3	A10
SW1-4	A11
SW1-5	A12
SW1-6	A13
SW1-7	A14
SW1-8	A15
SW2-1	A16
SW2-2	A17
SW2-3	A18
SW2-4	A19
SW2-5	A20
SW2-6	A21
SW2-7	A22
SW2-8	A23
SW3-1	A24
SW3-2	A25
SW3-3	A26
SW3-4	A27
SW3-5	A28
SW3-6	A29
SW3-7	A30
SW3-8	A31

TABLE 2

SWTICH DEFINITIONS

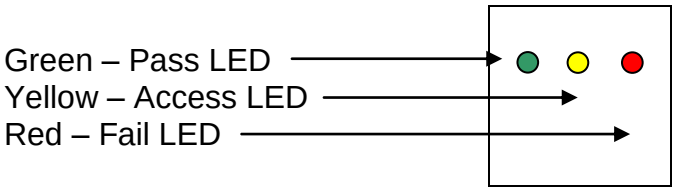
SW4-1	SW4-2	Address Modifiers	Address Space
Closed	Closed	09, 0D	Extended
Open	Closed	39, 3D	Standard
Closed	Open	29, 2D	Geographical *
Open	Open	29, 2D	Short

*Requires a special chassis

Front Panel LED Definitions

Three LED's are available at the front panel to indicate the board's status. The position of the LEDs is shown below.

Top of Front Panel



The Fail LED powers up on, and is controlled with bit 0 of the control register. Writing a one to bit 0 will turn off this LED. The state of this LED is reflected in bit 0 of the status register. When the Fail LED is on, and J1 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the control register. This LED will be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the status register reflects the state of this LED. Once the board has passed some initial power up tests this LED can be turned on to indicate successful completion of the power up sequence. The yellow, access LED will turn on anytime the board is accessed.

Connector Definitions

Two 96-position DIN connectors, (P1 and P2) are installed on the backplane end of the board to make the standard VME bus connection. The analog output signals and the external power supply connection are made through the a and c rows of the P2 connector. An optional DB37 female connector, installed through the board's front panel, is available to provide front access to the eight analog output channels.

The pin definitions of P2 and the DB37 connector are defined below and on the following page.

TABLE 3

P2 Connector

AGND	P2a1	P2c1	OUTPUT 0
AGND	P2a2	P2c2	OUTPUT 1
AGND	P2a3	P2c3	OUTPUT 2
AGND	P2a4	P2c4	OUTPUT 3
AGND	P2a5	P2c5	OUTPUT 4
AGND	P2a6	P2c6	OUTPUT 5
AGND	P2a7	P2c7	OUTPUT 6
AGND	P2a8	P2c8	OUTPUT 7
AGND	P2a9	P2c9	EXT V+
AGND	P2a10	P2c10	EXT V-

TABLE 4

DB37 CONNECTOR

		19	N/C
AGND	37		
		18	N/C
AGND	36		
		17	N/C
AGND	35		
		16	N/C
AGND	34		
		15	N/C
AGND	33		
		14	N/C
AGND	32		
		13	N/C
AGND	31		
		12	N/C
AGND	30		
		11	N/C
AGND	29		
		10	OUTPUT 0
AGND	28		
		9	OUTPUT 1
AGND	27		
		8	OUTPUT 2
AGND	26		
		7	OUTPUT 3
AGND	25		
		6	OUTPUT 4
AGND	24		
		5	OUTPUT 5
AGND	23		
		4	OUTPUT 6
AGND	22		
		3	OUTPUT 7
AGND	21		
		2	EXTV+
AGND	20		
		1	EXTV-

III. PROGRAMMING INFORMATION

The 9818/AO card responds to word and longword writes to the eight Digital to Analog Converters (DAC's). The card also supports word writes and reads to the control and status register, and word reads of the board identifier PROM. A thirty two-bit test register is provided, and it responds to word and longword transfers. This register is useful for verifying the functionality of the VME bus interface. The card's memory map is shown below.

TABLE 5

PAS 9818/AO MEMORY MAP

00	00	V (56)	01
02	00	M (4D)	03
04	00	E (45)	05
06	00	I (49)	07
08	00	D (44)	09
0A	00	P (50)	0B
0C	00	A (41)	0D
0E	00	S (53)	0F
10	00	9 (39)	11
12	00	8 (38)	13
14	00	1 (31)	15
16	00	8 (38)	17
18	00	A (41)	19
1A	00	O (4F)	1B
1C	00	A (41)	1D
1E	00	0 (30)	1F
20	98	18	21
22	Reserved	Control & Status	23
24	Reserved	Reserved	25
26	Reserved	Flag Register	27
28	Test Register	Test Register	29
2A	Test Register	Test Register	2B
2C	Reserved	Reserved	2D
3E	Reserved	Reserved	3F
40	CH 0	CH 0	41
42	CH 1	CH 1	43
44	CH 2	CH 2	45
46	CH 3	CH 3	47
48	CH 4	CH 4	49
4A	CH 5	CH 5	4B
4C	CH 6	CH 6	4D
4E	CH 7	CH 7	4F

Board Identifier PROM (Base + 001H to 01FH) Read Only

The Board Identifier PROM is located starting at the board's base address plus 1, and continues to the base address plus 1F. Byte and word reads to the Identifier PROM are supported.

Only the least significant byte of a word read will contain valid data, and the most significant byte will contain FF. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

Fast ID Register (Base Address + 20H) Read Only

The fast ID register is located at the boards base address plus 20 hex. Reads to this register will return the hex value 9818, which is the board's model number. Writing to this register will handshake, but not transfer any data.

Control and Status Register (Base +22H) Read / Write

The Control and Status Register (CSR) is located at the cards base address plus 22. Writes to the control register are used to set the states of the LED's and the SYSFAIL line, to control the simultaneous update function, and to software reset the board. The word format of the CSR is shown below.

TABLE 6

Control and Status Register

15	14 thru 5	4	3	2	1	0
Loop Back HT	Loop Back HT	Loop Back HT	SW Reset Pulse	Sim Updat HT	Pass LED HT	Fail LED LT

LT = Low True
HT = High True

Bit 0 of the CSR steers the Fail LED and the SYSFAIL line on the backplane, if JP2 is installed. When the card is reset the Fail LED will come on, and the SYSFAIL line will be driven true. Writing a one to bit 0 will turn off the LED and the SYSFAIL line.

Bit 1 of the CSR controls the Pass LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 will turn on the LED.

Bit 2 of the CSR controls the simultaneous update feature. This function is disabled when the board is reset or when a zero is written to bit 2. When simultaneous update is disabled, the DAC outputs will updated when they are written.

Simultaneous update is used to update all of the DAC outputs at the same time, and is controlled with bit 2. The program sequence for updating the outputs simultaneously is described below in the section on the D to A converters.

Bit 3 of the CSR is used to generate a software reset pulse when it is written with a one. Writing a zero to bit 3 causes no action. This bit will always return a 0 when read.

Bits 4 through 15 of the CSR are loop back bits, and will return the value that was last written to them.

The power up or reset condition of the CSR is 0000, and indicates, that simultaneous update is disabled, the Pass LED is off and the Fail LED is on.

Flag Register (Base + 26) Read Only

The Flag Register is located at the card's base address plus 26. This register provides access to the over-current flag outputs of the output amplifiers. Under normal operation all eight bits of this register should be zeros. Any bit that returns a one indicates the amplifier associated with that bit is in a fault condition. The word format of this register is shown below.

TABLE 7

Flag Register

15-8	7	6	5	4	3	2	1	0
All zero	Flag CH7	Flag CH6	Flag CH5	Flag CH4	Flag CH3	Flag CH2	Flag CH1	Flag CH0

Test Register (Base + 28) Read / Write

The 32-bit Test Register can be written to and read at the card's base address plus 28 (hex). This register supports word and long word transfers, and is useful for verifying the proper operation of the VME bus interface. Reading the register will return the value that was last written to it. System reset or software reset will clear this register to all zeros.

D to A Converters (Base + 40) Read/Write

The eight Digital to Analog Converters, (DAC's), are addressed starting at the board's base address plus 40 (hex). Binary Two's Complement is the data format written to the DAC's. Writing a value of 7FFF (hex) to a DAC produces positive full-scale output on that channel. Writing a value of 8000 (hex) produces negative full-scale output, and 0000 (hex) produces zero output.

Dual rank register pairs are used in the DAC's so that they can be updated simultaneously. Data is always written into the DAC's input register, which is the first register in the pair. If the simultaneous update feature is disabled, the second register, known as the DAC register, will also be updated during the write. This causes the output voltage for that channel to change immediately during the write. The board contains a set of eight sixteen-bit registers that shadow the values written to the DAC's input registers. These registors can be read back to determine the value that was last written to the DAC registers. Reading these addresses reads a register inside the EPLD, and does not read the DAC register. A system reset or software reset will clear all the DAC registers, and shadow registers to all zeros, and cause the output current to go to zero mAmps.

When the DAC's are updated simultaneously, all of the DAC input registers are written, then the card is instructed to update all the DAC registers. This causes all of the outputs to change at the same time.

The following sequence is performed to cause the outputs to update simultaneously;

1) Bit 2 in the CSR is set to a one to disable the DAC registers from tracking the input registers,
2) All of the DAC ‘s but one are written to,
3) Bit 2 in the CSR is set to zero,
4) The final DAC is written to. This will cause all of the DAC’s to be updated on the final write.

The Digital to Analog Converters can be written individually using word transfers, or in pairs using longword transfers. After a power up or software reset, the output voltage of all of the DAC’s is 0.000 mAmp.

IV. Power Dissipation and Power Supply Requirements

The output stage of the 9818/AO card uses two operational amplifiers. The main power amplifier supplies the current to the load, and the sense amplifier monitors the current and provides feedback to maintain the correct output. Both of these amplifiers are connected to the same high voltage power supplies, which are in the range of +/-10 volts to +/- 40 volts. Both amplifiers require a quiescent current even under no-load conditions that totals 11 mAmps per channel. The quiescent current of the output amplifier is 6 mAmps and the sense amplifiers require 5 mAmps per channel.

In order to calculate the power dissipated by the main amplifiers, the quiescent power is added to the power dissipated by output driver circuit; as shown in the following expression.

P (Total) = P (Quiescent) + P (Output Stage)

The maximum power will occur when the power supply voltage is at its maximum of +/-40 volts. In this case 80 volts x 6 mAmps produces 0.48 watts of quiescent power. The power in the output stage is equal to the voltage across the amplifier, times the maximum output current. Since a 50-ohm resistor is used to sense the output current, the voltage drop across this resistor is subtracted from the power supply voltage. At 40 mAmps of output current, two volts are dropped across the sense resistor. This leaves 38 volts across the output stage and the load. Under worst-case conditions, the load resistance would be near zero ohms so the entire 38 volts would drop across the output stage. This produces 38 volts x 40 mAmps = 1.52 watts of power in the output stage. The total power in the amplifier is 1.52 watts + 0.48 watts = 2.00 watts.

The output amplifiers use heat sinks that provide a junction to air thermal resistance of $25^{o}C/W$. The junction temperature of the amplifier should never exceed $125^{o}C$, and is calculated by adding the ambient temperature to the temperature rise caused by the power dissipation. The following expression defines this temperature: $T_J = T_A + P_D\Theta_{JA}$. In the case of this example with an ambient temperature of $60^{o}C$, the junction temperature would be; $T_J = 60^{o}C$ + 2 Watts x $25^{o}C/W = 110^{o}C$. This is below the maximum junction temperature, so it is safe to operate the amplifier under these conditions.

Several methods can be used to power the DACs and the output amplifiers. The DACs require a power supply voltage of +/-12 volts to +/-15 volts. This voltage can either be supplied by the +/-12 volt lines in the VME bus, or by on-board DC-to-DC converters, that step up the +5 volts from the backplane. The amplifiers require power supply voltages in the range of +/-10 volts to +/-40 volts. These voltages can either be supplied externally or by on-board DC-to-DC converters.

Two configurations of DC-to-DC converters are available as options. In each case, two dual output supplies are used that provide either +/-12 volts or +/-15

volts times two. Using the +/-24 volt configuration, the DACs are powered with +/-12 volts and the amplifiers are powered with +/-24 volts. The +/-30 volt configuration powers the DACs with +/-15 volts and the amplifiers with +/-30 volts.

The DACs each require a quiescent current of 15 mAmps of +12 to +15 volts and 25 mAmps of –12 to –15 volts. This produces a total current requirement for all of the DACs on-board of 120 mAmps from the positive supply and 200 mAmps from the negative supply. This current can either be supplied from the +/-12 volt backplane voltage or the on-board DC-to-DC converters.

The amplifier circuits each require 11 mAmp of quiescent current for a total of 88 mAmps for the entire board. This current can either be supplied by external supplies or by the on-board DC-to-DC converters.

When the DC-to-DC converters are used, two dual output power supplies are configured to provide the four voltages for the DACs and the amplifiers. In this configuration the quiescent current for the DACs and the amplifiers must be added together. The following table shows the output current and voltage from the DC-to-DC converters and the amount available to deliver to the load.

TABLE 8

Power Supply Data

	+/-24 Volt Option	+/-30 Volt Option
DAC Voltage	+/-12 volts	+/-15 volts
Amplifier Voltage	+/-24 volts	+/-30 volts
Positive PS Current	625 mAmps	500 mAmps
Negative PS Current	625 mAmps	500 mAmps
Positive Quiescent I	208 mAmps	208 mAmps
Negative Quiescent I	288 mAmps	288 mAmps
Positive Load Current	417 mAmps	292 mAmps
Negative Load Current	337 mAmps	212 mAmps

Since each amplifier can deliver +/-40 mAmps to the load, the total load current could be as high as 320 mAmps. It can be seen from the table that the +/-24 volt power supply option has the capability of delivering this amount of current, and the +/-30 volt option does not. The 30-volt option is still useful for driving higher impedance loads. A 1.2K ohm load driven with 20 mAmps would produce 24 volts across the load, and could be powered with the 30 volt supplies and not the 24 volt supplies. For loads that require higher output currents and voltages, the external power supply option is available.

V. CALIBRATION PROCEDURE (+/-40 mAmp)

Install the 9818/AO card in a VME chassis, and connect the external power supply to the card (if required). Allow the card to stabilize for approximately 15 minutes.

Offset Adjustment

The offset adjustment is performed before the gain adjustment to avoid interaction of adjustments. Write the hex value 8000 to the channel being calibrated, and adjust the zero potentiometer for a value of 40.0000 mAmps. The zero adjustments are defined in the Table 9, below.

Gain Adjustment

Write a hex value of 7FFF to the channel being calibrated, and adjust the gain potentiometer for a value of + 39.9988 mAmps. The gain adjustments are the defined in Table 9, below. Write the hex value 0000 to the channel being calibrated and verify the output current is 0.0000 mAmps.

TABLE 9

OFFSET AND GAIN ADJUSTMENT POTS

Channel Number	P3 Pin Number	Offset Pot	Gain Pot	Channel Address
0	10	R39	R36	40
1	9	R15	R12	42
2	8	R45	R42	44
3	7	R21	R18	46
4	6	R51	R48	48
5	5	R27	R24	4A
6	4	R57	R54	4C
7	3	R33	R30	4E