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PAS 9883/GEN
ENGINEERING SPECIFICATION

EIGHT CHANNEL VME SYNCHRONIZED SINE/PULSE GENERATOR CARD
Rev B1 (08/25/10)

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Eight Channel VME
Sine/Pulse Generator Card

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Sine/Pulse Generator Card

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I. INTRODUCTION

GENERAL DESCRIPTION

The PAS 9883/GEN is a VME based, eight channel function generator card. Each channel contains a Direct Digital Synthesis (DDS) chip that can be programmed to generate sine wave output signals. This DDS device is a Numerically Controlled Oscillator (NCO), employing a phase accumulator, a sine look-up table and a 10 bit D/A converter. The input clock frequency to the DDS chips is 2 MHz. This input frequency combined with the chips thirty-two bit phase accumulator provides a frequency resolution of 0.000465 Hz. The maximum useable output frequency is approximately 30 KHz.

A Multiplying Digital-to-Analog Converter (MDAC) is provided on each channel, following the DDS. This allows the card's output voltage to be set from 0 to +/-10 volts in 5 mV steps. In addition to the sine wave output a TTL output and open drain FET output are provided on each channel.

This card can be used in VME systems with A16, A24, or A32 addressing, and data bus widths of 16 and 32 bits are supported. DIP switches are used to configure the width of the address bus. VME instruction types determine the width of the data bus. The output signals are connected to a pair of DB37 female connectors mounted through the front panel. A board identifier PROM, control register and DDS frequency and phase control registers are provided as well.

Card Features: PAS 9883/GEN

- 8 channel Direct Digital Synthesis (DDS) Waveform Generator
- Each channel provides sine wave, TTL square wave and open drain FET outputs
- Multiplying Digital-to-Analog Converter (MDAC) per channel provides output voltage of 0 to +/-10 volts in 4.88 mV steps
- Output frequency is controlled by a 32 bit frequency register; each channel provides an independent frequency register
- Output frequency is set by the following equation: F(out) = F register value x 2 MHz divided by 2^32
- Each channel's output phase is controlled by two independent 12 bit phase offset registers
- All channels are clocked by a common 2 MHz crystal controlled oscillator
- All channels can be synchronized, to allow known phase offset from channel to channel
- Sine wave output amplifiers provide a low pass filter with a 3dB corner frequency of 30 KHz
- VME 6U form factor, 233mm x 160mm card size
- VME access: A32, A24, A16; D16 slave – No VME interrupts
- Board provides ID code (VMEIDPAS9883GENA), control and status register and three status LEDs
- Operating temperature range 0 to 60 degrees Celsius

II. SPECIFICATIONS

Electrical Specifications

General Information

Number of Sine/Pulse Out Channels	8
DDS Component	Analog Devices PN: AD9831 (see data sheet for additional info)

Output Characteristics

Sine Outputs

Voltage Ranges	0 to +/-10 Volts in 4.88 mV steps
Output Current	+/-15 mA (typ)
Short-Circuit Current	+/-40 mA (typ)
Low Pass Corner Frequency	31 KHz

TTL Outputs

Low Level Output Current	10 mA
High Level Output Current	-10 mA
Low Level Output Voltage @ IOL = 4 mAmps	0.40 V (typ.), 0.6 V (max.)
High Level Output Voltage @ IOH = -1 mA	3.6 V (min.), 3.9 V (typ.)
High Level Output Voltage @ IOH = -10 mA	3.4 V (min.), 3.8 V (typ.)

FET Outputs

Pull-up Resistor	1k Ohms
Pull-up Voltage	+30 Volts (max)
Sink Current	100 mA (typ)

Card Power Requirements	5 Volts @ 1 Amp (typ)
VMEbus Compliance	Fully compatible with VMEbus standard
Address Range	A32, A24, and A16 switch selectable
Address Block Size	256 consecutive byte locations
Data Width	D16
Interrupts	none

Environmental Specifications

Operating Temperature Range	0 to 60 degrees Celsius
Storage Temperature Range	-40 to 85 degrees C.
Relative Humidity Range	0% to 100%, non-condensing

Physical Specifications

Dimensions	Form factor: 6U (160 mm x 233 mm)
Weight	12 oz. (typ)
Connectors	2 ea. 96 pos. DIN (VME bus connectors) 2 ea. DB37 female (Sine/Pulse Outputs) 1 ea. 6 pin shrouded header (reference and power supply voltages) Mating connector = Molex p/n 50-57-9406

Switches and Jumper Plug Definitions

The PAS 9883/GEN card contains three eight position DIP switches, one three position DIP switch, and ten jumper plugs. The three eight position DIP switches are used to set the card's VME address and are defined in Table 1 on page 10. When a switch is closed, the corresponding address bit must be low to select the card's address, and when a switch is open, the corresponding address bit must be high.

Switches SW4-1and 2are used to select the card's operating environment; A16, A24, or A32. The setting of these switches is defined in Table 2 on page 11. SW4-3 has no function at this time.

The card is shipped configured for address 1000 in short space.

Jumper plugs 2 and 3 control SYSFAIL and the source of the master clock as described in the table 3. The card is shipped with JP2 installed, so that SYSFAIL is controlled by the CSR. JP3 is installed from 1 to 2 so that SYSCLK provides the master clock.

Jumper plugs JP4 through JP11 are used to select the source of the pull up voltage for the open drain FET output on channels 1 through 8 respectively. When the jumpers are in position 1 to 2, the pull up resistors are connected to the external voltage pins in the DB37 connectors. When the jumpers are in position 2 to 3, the pull up resistors are connected to the +15 volt power supply.

The card is shipped with the pull-up jumpers in position 2 to 3 to select the +15 Volt power supply.

TABLE 1

DIP Switch Definitions

Switch #	Function
SW1-1	A8
SW1-2	A9
SW1-3	A10
SW1-4	A11
SW1-5	A12
SW1-6	A13
SW1-7	A14
SW1-8	A15
SW2-1	A16
SW2-2	A17
SW2-3	A18
SW2-4	A19
SW2-5	A20
SW2-6	A21
SW2-7	A22
SW2-8	A23
SW3-1	A24
SW3-2	A25
SW3-3	A26
SW3-4	A27
SW3-5	A28
SW3-6	A29
SW3-7	A30
SW3-8	A31

TABLE 2

Switch Definitions

SW4-1	SW4-2	Address Modifiers	Address Space	# Of Bits
Closed	Closed	09, 0D	Extended	32 bit
Open	Closed	39, 3D	Standard	24 bit
Closed	Open	29, 2D	Geographical*	16 bit
Open	Open	29, 2D	Short	16 bit

* Requires a special chassis

TABLE 3

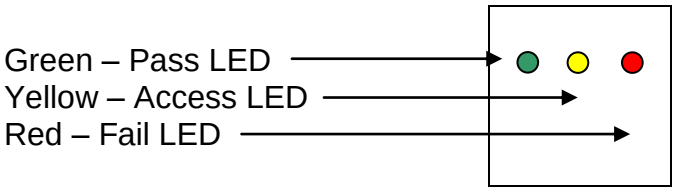
Jumper Definitions

Jumper	Function
JP1	Reserved for future use
JP2	SYSFAIL controlled by control register
JP3, 1-2	Use SYSCLK as master 16 MHz clock
JP3, 2-3	Use on-board 16 MHz oscillator
JP4	Channel 1 Pull-up Voltage Select
JP5	Channel 2 Pull-up Voltage Select
JP6	Channel 3 Pull-up Voltage Select
JP7	Channel 4 Pull-up Voltage Select
JP8	Channel 5 Pull-up Voltage Select
JP9	Channel 6 Pull-up Voltage Select
JP10	Channel 7 Pull-up Voltage Select
JP11	Channel 8 Pull-up Voltage Select

Front Panel LED Definitions

Three LED's are available at the front panel to indicate the board's status. The position of the LEDs is shown below.

Top of Front Panel



The Fail LED powers up on, and is controlled with bit 0 of the control register. Writing a one to bit 0 will turn off this LED. The state of this LED is reflected in bit 0 of the status register. When the Fail LED is on, and JP2 is installed, the SYSFAIL line will be driven on the VMEbus.

The Pass LED is controlled by bit 1 of the control register. This LED will be turned on by writing a one to bit 1, and it will power up turned off. Bit 1 in the status register reflects the state of this LED. Once the board has passed some initial power up tests this LED can be turned on to indicate successful completion of the power up sequence. The yellow, access LED will turn on anytime the board is accessed.

Connector Definitions

Two 96 position DIN connectors are installed on the backplane end of the board to make the standard VME bus connection. A pair of DB37 female connectors is installed through the board's front panel to provide access to eight sine/pulse output channels. A six position shrouded header is provided between the DB37 connectors to provide access to the reference voltages and power supplies. The pin out of these connectors is defined below and on the following page.

TABLE 4

6 Position Shrouded Header, P6

Pin #	Signal Name
1	Reference Voltage High
2	Analog Ground
3	-0.500 Volts
4	+15 VA
5	Analog Ground
6	-15 VA

TABLE 5

DB37 Connectors

			(P4)	(P3)
		19	AGND	AGND
AGND	37			
		18	EXTV4	EXTV8
GND	36			
		17	HV04	HV08
GND	35			
		16	TTL4	TTL8
GND	34			
		15	SINE4	SINE8
AGND	33			
		14	EXTV3	EXTV7
GND	32			
		13	HV03	HV07
GND	31			
		12	TTL3	TTL7
GND	30			
		11	SINE3	SINE7
AGND	29			
		10	EXTV2	EXTV6
GND	28			
		9	HV02	HV06
GND	27			
		8	TTL2	TTL6
GND	26			
		7	SINE2	SINE6
AGND	25			
		6	EXTV1	EXTV5
GND	24			
		5	HV01	HV05
GND	23			
		4	TTL1	TTL5
GND	22			
		3	SINE1	SINE5
AGND	21			
		2	AGND	AGND
AGND	20			
		1	AGND	AGND

III. PROGRAMMING INFORMATION

The PAS 9883/GEN card responds to word transfers to the control register set. The card's memory map is shown below, and occupies 256 bytes of VME memory.

TABLE 6

PAS 9883/GEN MEMORY MAP

BASE A+000	00	V (56)	001
002	00	M (4D)	003
004	00	E (45)	005
006	00	I (49)	007
008	00	D (44)	009
00A	00	P (50)	00B
00C	00	A (41)	00D
00E	00	S (53)	00F
000	00	9 (39)	011
012	00	8 (38)	013
014	00	8 (38)	015
016	00	3 (33)	017
018	00	G (47)	019
01A	00	E (45)	01B
01C	00	N (4E)	01D
01E	00	A (41)	01F
020	98	83	021
022	CONTROL & STATUS	CONTROL & STATUS	023
024	RESERVED	RESERVED	025
03E	RESERVED	RESERVED	03F
040	MASTER PHASE/FREQ SELECT	MPFSR	041
050	Channel Control Register 1	CCR1	051
052	Channel Control Register 2	CCR2	053
054	Channel Control Register 3	CCR3	055
056	Channel Control Register 4	CCR4	057
058	Channel Control Register 5	CCR5	059
05A	Channel Control Register 6	CCR6	05B
05C	Channel Control Register 7	CCR7	05D
05E	Channel Control Register 8	CCR8	05F
060	RESERVED	RESERVED	061
07E	RESERVED	RESERVED	07F
080	CHANNEL 1	FREQ 0 REG 16 LSBs	081
082	CHANNEL 1	FREQ 0 REG 16 MSBs	083
084	CHANNEL 1	FREQ 1 REG 16 LSBs	085
086	CHANNEL 1	FREQ 1 REG 16 MSBs	087
088	CHANNEL 1	PHASE 0 REG	089
08A	CHANNEL 1	PHASE 1 REG	08B
08C	CHANNEL 1	PHASE 2 REG	08D
08E	CHANNEL 1	PHASE 3 REG	08F
090	CHANNEL 2	REGISTER SET	09F
0A0	CHANNEL 3	REGISTER SET	0AF
0B0	CHANNEL 4	REGISTER SET	0BF
0C0	CHANNEL 5	REGISTER SET	0CF
0D0	CHANNEL 6	REGISTER SET	0DF
0E0	CHANNEL 7	REGISTER SET	0EF
0F0	CHANNEL 8	REGISTER SET	0FF

Board Identifier PROM (Base Address + 001H to 01FH) Read Only

The Board Identifier PROM is located starting at the board's base address plus 1, and continues to the base address plus 1F.

Byte and word reads to the Identifier PROM are supported. Only the least significant byte of a word read will contain valid data, and the most significant byte will contain OO. The ID PROM contains 16 ASCII characters that specify the board's model number and revision level. A write to the ID PROM location will handshake, but not transfer any data.

Fast ID Register (Base Address + 20H) Read Only

The fast ID register is located at the card's base address plus 20. Reads to this register will return the hex value 9883, which is the board's model number. Writing to this register will handshake, but not transfer any data.

Control & Status Register (Base Address + 22H) Read / Write

The Control & Status Register, (CSR), provides four bits that are used to set the states of the front panel LED's, enable the 2 MHz clock signal, select the DDS control mode and reset the board. The format of this register is shown below.

TABLE 7

Control & Status Register

15	14 - 5	4	3	2	1	0
Loop Back	Loop Back	DDS Reset	Select DDS Control	2 MHz Enable	Pass LED	Fail LED

Bit 0 of the CSR steers the Fail LED at the front panel. The SYSFAIL line on the backplane will also be asserted if JP2 is installed, and bit 0 is reset. When the card is reset the Fail LED will come on. Writing a one to bit 0 will turn off the LED and the SYSFAIL line. Reading bit 0 returns the state that was last written.

Bit 1 of the CSR controls the Pass LED. This LED will be turned off when the board is reset or when a zero is written to bit 1. Writing a one to bit 1 will turn on the LED. Reading bit 1 returns the state that was last written.

Bit 2 of the CSR enables the 2 MHz clock signal to the DDS generator chips. This bit powers up reset, so it must be written to a one in order for the card to generate any output signals. Reading this bit returns the value that was last written.

Bit 3 of the CSR determines how the DDS phase and frequency control registers will be selected. When this bit is a zero, the phase and frequency select functions will be controlled by the individual channel control registers. When this bit is a one, the phase and frequency select functions will be controlled by the master phase / frequency select registers.

Bit 4 of the CSR controls the DDS reset function. Writing a one to bit 4 will reset the DDS chips with a pulse. The only effect this has on the DDS chips is to reset all the phase accumulators to zero, which synchronizes all of the outputs with respect to each other. Reading bit 4 will always return a value of zero.

Bit 5 through 15 of the CSR will return the value that was last written. These bits have no other functions.

Master Phase / Frequency Select Register (Base Address + 041) Read / Write

The Master Phase / Frequency Select Register (MPFSR) is used to select which phase and frequency control registers are being used in the DDS chips. This register controls all of the DDS chips with a single instruction, and allows a known phase relationship between channels to be maintained. In order to use this register, it must be selected by setting bit three of the CSR to a one. The format of this register is shown below

TABLE 8

Master Phase / Frequency Select Register

15	14	13	12	11 ——— 4	3	2	1	0
Phase Select CH 8	Freq Select CH 8	Phase Select CH 7	Freq Select CH 6	Phase & Freq Select Ch 5 - 3	Phase Select CH 2	Freq Select CH 2	Phase Select CH1	Freq Select CH 1

Bit 0 of the MPFSR is used to select which register controls the output frequency of channel one. Each DDS chip has 2, 32 bit frequency control registers. When bit 0 is a zero, frequency register zero is selected. When it is a one, frequency register one is selected. Reading this bit will return the value last written.

Bit 1 of the MPFSR is used to select which register will be used to control the phase offset of channel one. Each DDS chip has four, 12 bit phase offset registers. This card only provides access to two of the phase offset registers. When bit 1 is a zero it selects phase register zero, and when it is a one, selects phase register one. Reading this bit will return the value last written.

The remaining bits in this register control the phase and frequency select registers of channels 2 through 8. Reading this register will return the value last written.

Channel Control Registers (Base Address + 051 thru 05F) Read / Write

The Channel Control Registers (CCR) are used to set the gain of the output amplifier, and to select the source of the frequency and phase offset registers. The format of these registers is shown below.

TABLE 9

Channel Control Register

15	14	13	12	11	10-1	0
Phase Select	Freq Select	Loop Back	Loop Back	MDAC MSB	MDAC 10-1	MDAC LSB

Bit 0 and 11 of the CCR of the CCR contain the value that controls the Multiplying Digital-to-Analog Converter (MDAC). Writing all ones to this register will cause the output sine wave to be the maximum value of +/- 10 Volts. Writing a smaller value to this register will cause a proportionally smaller output voltage. The LSB bit weight is 4.88 mVolts. Reading these bits back will return all ones.

Bit 12and 13 of the CCR are loop-back bits and have no other function. Reading these bits will return the value last written.

Bit 14 of the CCR is used to select which register controls the output frequency when it is enabled by bit 3 of the CSR being a zero. Each DDS chip has two, 32-bit frequency control registers. When bit 14 is a zero it selects frequency register zero, and when it is a one, selects frequency register one. Reading this bit will return the value last written.

Bit 15 of the CCR is used to select which register will be used to control the phase offset, when it is enabled by bit 3 of the CSR being a zero. Each DDS chip has four, 12-bit phase offset registers. This card only provides access to two of the phase offset registers. When bit 15 is a zero it selects phase register zero, when it is a one, selects phase register one. Reading this bit will return the value last written.

Frequency Control Registers / Write Only (Base Address + 080–087, 090–097, 0A0–0A7, 0B0–0B7, 0C0–0C7, 0D0–0D7, 0E0–0E7, 0F0–0F7)

Each DDS chip contains two, 32-bit frequency control registers. The output frequency is determined by the value in the frequency register divided by 2^32 and multiplied by 2 MHz. The register that is used to set the frequency is determined by bit 14 in the CCR or by the master phase/frequency register. In order to generate output frequencies, bit 2 in the CSR must be set to a one in order to enable the 2 MHz clock source to the DDS chips.

Phase Control Registers / Write Only (Base Address + 088–08F, 098–09F, 0A8–0AF, 0B8–0BF, 0C8–0CF, 0D8–0DF, 0E8–0EF, 0F8–0FF)

Each DDS chip contains four, 12 bit phase control registers. This card only allows selecting phase offset registers zero and one. The register that is used to set the phase is determined by bit 15 in the CCR or by the master phase/frequency registers. These registers can be used to modulate the phase of the output waveform.

IV. CALIBRATION PROCEDURE

Install the PAS 9883/GEN card to be calibrated in a VME chassis and apply power.

Connect the positive lead of a precision DVM to TP1 and the negative lead to TP2 and adjust R153 for 1.300 Volts.

Move the positive lead to TP3 and adjust R150 for –0.510 Volts.

Write the following values to the cards control registers.

TABLE 10
Control Register Values

Offset	Value	Offset	Value	Offset	Value
22	000F	A0	0000	E0	0000
		A2	0020	E2	0020
40	0000	A4	0000	E4	0000
		A6	0020	E6	0020
50	0FFF	A8	0000	E8	0000
52	0FFF	AA	0400	EA	0C00
54	0FFF				
56	0FFF	B0	0000	F0	0000
58	0FFF	B2	0020	F2	0020
5A	0FFF	B4	0000	F4	0000
5C	0FFF	B6	0020	F6	0020
5E	0FFF	B8	0000	F8	0000
		BA	0600	FA	0E00
80	0000				
82	0020	C0	0000		
84	0000	C2	0020		
86	0020	C4	0000		
88	0000	C6	0020		
8A	0000	C8	0000		
		CA	0800		
90	0000				
92	0020	D0	0000		
94	0000	D2	0020		
96	0020	D4	0000		
98	0000	D6	0020		
9A	0200	D8	0000		
		DA	0A00		

The first write to the CSR turns off the fail LED, turns on the pass LED, enables the 2 MHz clock and sets the phase and frequency registers to be selected by the master phase/frequency select register.

The write at address 40 to the master phase/frequency select register, selects register zero for phase and frequency select on each channel.

The writes from 50 to 5E of 0FFF, sets all channels MDACs to full scale +/- 10 Volt outputs.

The writes from 80 to 86 loads both frequency registers on the first channel to 0020 0000. This corresponds to a frequency of approximately 1 KHz. The writes to 88 and 8A select no phase offset to channel zero.

The writes to the registers from 90 to FA set the frequency of all channels to approximately 1 KHz and points the first phase register to zero offset and the second phase register to offset by 45 degrees from the previous channel.

Observe the sine wave output of channel 1, (P4-3), with an oscilloscope to be a +/- 10 V peak to peak sine wave with a frequency of approximately 1 KHz. Observe the remaining 7 channels with another channel of the oscilloscope to be the same frequency and amplitudes as channel 1, but with a random phase relationship.

Write a 1F to the CSR (offset 22) to reset the phase accumulators and verify that all 8 are now in sync with no phase shift.

White an FFFF to the MPFSR (offset 40) and observe the phase shifts by an additional 45 degrees for each incremental channel.

Verify all the TTL and high voltage outputs with the scope.

Connect the DVM set for DC Volts from channel 1 sine wave output to analog ground, and adjust R26 for 0 mV, +/- 2 mV.

Connect DVM set for AC Volts from channel 1 sine wave output and adjust R21 for 7.070 Volts AC +/- 2 mV.

Repeat for the remaining channels. Table 11 on page 21 defines the zero and gain pots for each channel.

TABLE 11
Offset and Gain Adjustment Potentiometers

Channel	Output Pin	Zero Pot	Gain Pot
1	P4-3	R26	R21
2	P4-7	R42	R37
3	P4-11	R58	R53
4	P4-15	R74	R69
5	P3-3	R90	R85
6	P3-7	R106	R101
7	P3-11	R122	R117
8	P3-15	R138	R133